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Applications of selectively-doped two-dimensional electron layers

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(1. X. 1984)

In honor of Emanuel Mooser's 60th birthday

Abstract. The basic concepts and applications of selectively doped high electron mobility field effect transistors are reviewed. In these structures, the current flow is controlled by modulating the density of a 2-dimensional electron gas confined in a narrow potential well formed at the interface between semiconductors with different bandgaps. These devices show interesting properties whose study contributes to the understanding of electron transport and quantum effects in 2-dimensional systems, and also show promise for use in high-frequency low-noise analog amplification and ultrafast large scale integrated digital systems.

1. Introduction

Since the first demonstration in 1978 of high-mobilities achievable with selective (modulation) doping in GaAs–AlGaAs superlattices [1] and single interface heterojunctions [2], these structures have attracted great interest for their intrinsic physical properties and their potential application to high-speed devices. The study of these systems has yielded new insights into the electronic properties of two-dimensional ($2D$) electron gases, and has led, to the discovery of the fractional quantum Hall effect in very high mobility resistance standards [3].

The possible device applications of $2D$-electron gas systems in field effect transistors (FET's) and integrated circuits, have formed the focus of intense activity in many laboratories over the past 5 years. FET performances achieved to date already significantly exceed the best results obtainable with more conventional devices in terms of speed and power-delay product for both room temperature and 77 K operation [4–7], and it appears likely that these $2D$-devices will attain wide industrial importance for supercomputer, instrumentation, and microwave amplification applications.

The object of this paper is to briefly present the most significant features of $2D$-electron gas systems at semiconductor heterostructure interfaces and to illustrate the application of these concepts to field effect transistors. The presentation will be limited to the single differentially doped GaAs–AlGaAs interface case, although $2D$-behavior and enhanced mobilities have also been demonstrated in other systems such as GaInAs–InP [8] and GaInAs–AlInAs [9]. Crystal growth and processing aspects, based on the molecular beam, metal-organic, or conventional vapor phase epitaxy techniques, which have played a crucial role in

the development of the 2*D*-devices, will not be discussed here in view of the very extensive literature existing on the subject.

2. GaAs/AlGaAs interfaces: energy bands and doping considerations

The selectively doped GaAs/AlGaAs heterostructures derive their unique properties from the fact that carriers (electrons or holes) transfer from the highly doped–high bandcap AlGaAs to the lower bandgap undoped GaAs side of the interface where they are confined in a very narrow potential well and form a 2*D*-electron gas or -hole gas, respectively (Fig. 1). At low temperatures (<100 K), this degenerate 2*D*-carrier gas exhibits a markedly enhanced mobility compared to that observed in bulk GaAs layers, due to the spatial separation between free carriers and charged donors or acceptors with the concommittant reduction in ionized impurity scattering. The mobility of the 2*D*-gas is further enhanced by the insertion of an undoped AlGaAs spacer layer between the *n*- or *p*-type AlGaAs and the undoped GaAs, and maximum electron mobilities in excess of 10^6 cm^2/Vs have been attained [10–12].

The problem of calculating the sheet carrier concentration and electron mobility of the 2*D*-electron gas as a function of the doping density in AlGaAs, the thickness of the undoped spacer layer, the lattice temperature, and other device parameters, has been addressed by many authors [13–18]. The calculations

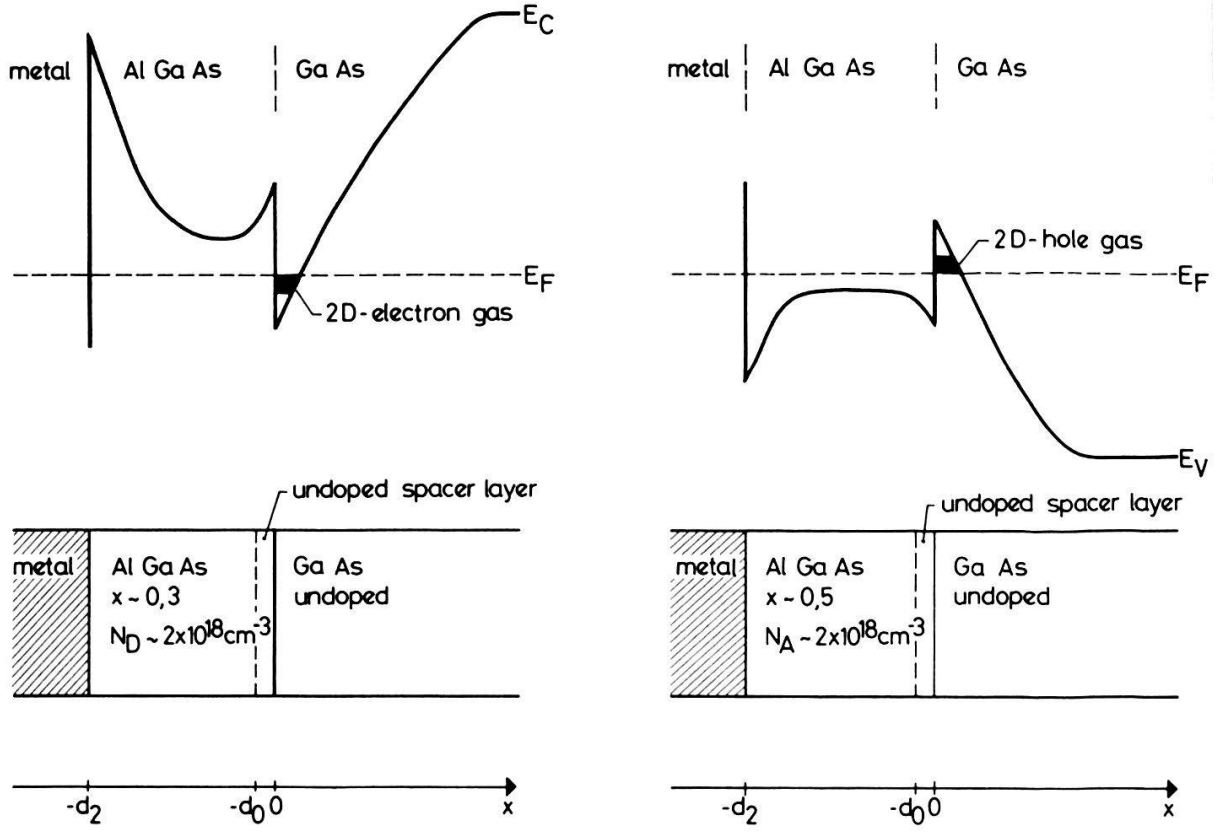

Figure 1
Schematic diagram of (a) the conduction band edge across a *N*-AlGaAs/GaAs and (b) the valence band edge across a *P*-AlGaAs/GaAs selectively doped interface with Schottky gate in thermal equilibrium. The thickness of the undoped AlGaAs spacer layer is denoted d_0 and it is assumed that the doped AlGaAs is sufficiently thick not to be completely depleted.

are similar to those for the inversion layer at silicon–silicon dioxide interfaces, with the main difference that the wave functions have a non-vanishing amplitude in AlGaAs because the interface barrier height is not infinitely large (~300 meV typically for GaAs–AlGaAs as compared to ~3.2 eV for Si–SiO_2). The smaller effective mass of electrons in GaAs further leads to a larger separation of the subbands in the $2D$-channel well for comparable electron densities. As a result, the GaAs–AlGaAs interface layer is more two-dimensional than a Si inversion layer and even at ~300 K, up to ~60% of the electrons are confined in the lowest subband at sheet densities $\sim 10^{12}\,\mathrm{cm}^{-2}$ (as compared to ~30% in Si). Finally, because of the lower density of states available in GaAs (single valley), the Fermi level tends to lie very close to or inside the allowed energy subbands, so that the Boltzmann approximation is no longer valid and Fermi statistics must be used to describe the level occupancy.

(a) *Self-consistent energy band calculation*

A self-consistent equilibrium energy band calculation for the GaAs–AlGaAs $2D$-system has first been presented by Ando [13], in which the potential for the electrons is determined by the solution of Poisson's equation using a depletion approximation and taking into account the conduction band discontinuity ΔE_c at the interface. The solution is based on the effective mass approximation, and the electron wave functions and their derivatives in GaAs and AlGaAs are connected at the interface through an appropriate interface matrix [13].

A somewhat simplified approach to the same problem has been presented more recently by Vinter [14], which takes into account the electronic subband structure in the $2D$-well, as well as the partial neutralization of donors in AlGaAs. The approach adopts a single wavefunction approximation throughout the heterostructure by neglecting the small differences in dielectric constant and electron effective mass between GaAs and AlGaAs materials. The potential for the electrons is then determined by self-consistent solution of Poisson's equation and the conduction band discontinuity ΔE_c at the interface, i.e.

$$d^2V/dx^2 = -(1/\varepsilon)\cdot\rho(x) \tag{1}$$

$$V(0^+) = V(0^-) + \Delta E_c/e \tag{2}$$

where 0 represents the interface coordinate, ΔE_c the conduction band discontinuity, and ρ the space charge density, the other symbols having their usual meaning. The space charge density is given by the ionized impurity distribution and the free electron density

$$\rho(x) = e[N_D^+(x) - n(x)] \tag{3}$$

where the ionization probability for the fixed charges is determined by Fermi statistics.

The electron wave functions are determined by solution of the effective mass Schrödinger equation

$$-(\hbar^2/2m)\cdot d^2\xi_n/dx^2 - eV(x)\cdot\xi_n(x) = E_n\cdot\xi_n(x) \tag{4}$$

where ξ_n is the wave function and E_n the energy at the bottom of subband n, and the total free electron concentration is then obtained by sommation over the

different subbands

$$n_s(x) = D \sum_n |\xi_n(x)|^2 N_n \tag{5}$$

where

$$D = m/\pi\hbar^2 \tag{6}$$

represents the $2D$-density of states, identical for the different subbands, and

$$N_n = kT \cdot \ln[1 + \exp(E_F - E_n)/kT] \tag{7}$$

the occupancy integral from Fermi statistics. In these expressions, the energy difference $(E_F - E_n)$ depends on the sheet electron density n_s, since the energy of the bottom of the subband n moves up or down with respect to the energy minimum $E_{\min}$ in the potential well as the electron concentration in the channel is varied. The Fermi energy, E_F, is considered constant in the x direction perpendicular to the channel in the absence of any gate to substrate current along x.

A self-consistent solution to equations (1) to (5) yields the potential variation $V(x)$ and electron distribution $n(x)$ throughout the system subject to the matching conditions at the boundaries. For the selectively doped two-dimensional electron gas field effect transistor (TEGFET) with Schottky barrier gate, illustrated schematically in Fig. 2, the boundary conditions for the potential are, at $x = -d_2$

$$V(-d_2) = V_{bi} - V_G \tag{8a}$$

where V_{bi} is the built-in barrier potential and V_G the applied gate voltage, and at $x = \infty$

$$V(\infty) = V_B \tag{8b}$$

where V_B is the potential in the undoped GaAs base layer far removed from the heterostructure interface.

The results of the self-consistent calculation are given in Fig. 3 (from ref. 14) for a TEGFET structure for 2 different values of V_G. At the lower gate voltage ($V_G = -1.5$ V), the AlGaAs layer is fully depleted of electrons and the conduction takes place only in the channel. At the higher gate voltage ($V_G = -0.5$ V), parallel conduction in the AlGaAs starts to become important and further increases in V_G mainly serve to raise the number of electrons in the AlGaAs.

The calculated electron density in the channel is displayed in Fig. 4 as a function gate voltage for the device of the previous figure. As expected, one

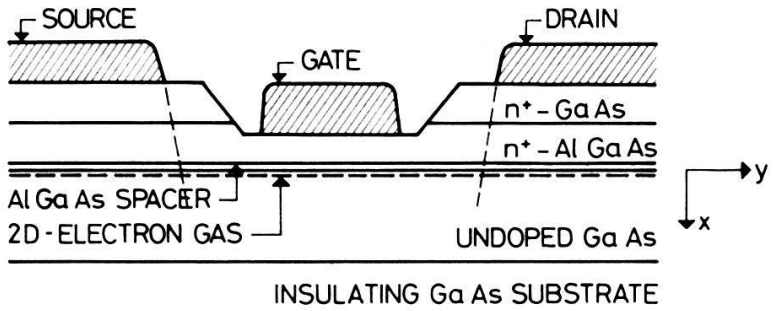

Figure 2
Schematic diagram of a selectively doped TEGFET structure with recessed Schottky gate.

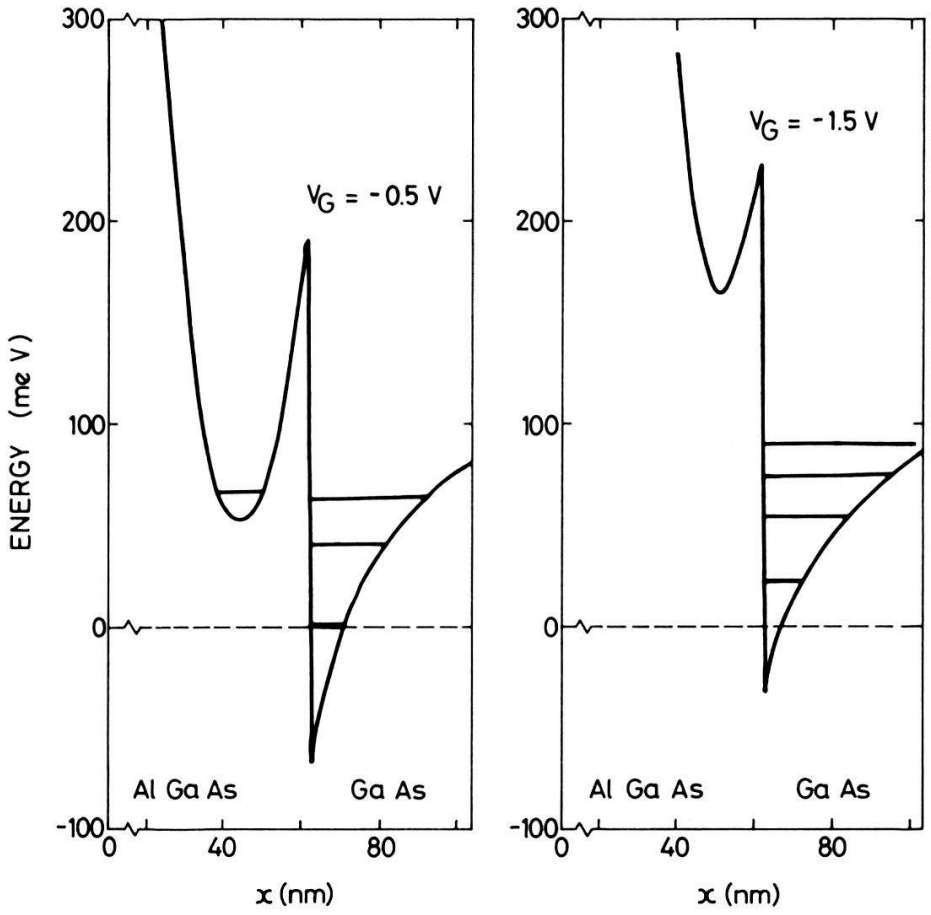

Figure 3
Self-consistent potential for conduction electrons in a depletion-mode TEGFET structure for two different gate voltages. AlGaAs electrons are shown quantized because of the narrowness of the potential well in AlGaAs. Device parameters: Al concentration $x = 0.26$, AlGaAs doping $N_{D2} = 1.3 \times 10^{18}\,\mathrm{cm}^{-3}$, donor binding energy $E_{D2} = 50$ meV, thicknesses $d_0 = 7.5$ nm, $d_2 = 55$ nm, conduction band discontinuity $\Delta E_c = 260$ meV, substrate potential $V_B = 1$ V, Schottky gate built-in potential $V_{bi} = 1$ V. (after Vinter [14]).

observes a range of gate voltages where the channel density n_s increases nearly linearly with V_G as is the case for Si metal-oxide FET's. At the high end of the linear range, the density of the high mobility electrons saturates, as the AlGaAs layer starts to populate, which limits the useful range of operation of the devices.

In many instances, it is not necessary to resort to a full consistent calculation and simpler approaches can be used to approximate the device behavior. The simpler models make it possible to obtain a solution in analytical form; they generally proceed by accounting for the $2D$-nature of the electrons in the channel in a phenomenological way [15–16], or by neglecting the wave function penetration in the high bandgap material as well as the subband structure in the well [17, 18]. These approaches yield good guidelines values and are useful to predict doping levels and spacer thicknesses to be used for optimum channel doping and mobility.

The model originally developed by Delagebeaudeuf and Linh [15] and which is based on the triangular well approximation and the hypothesis of full depletion in the AlGaAs and GaAs interface layers will be discussed next as a generic example.

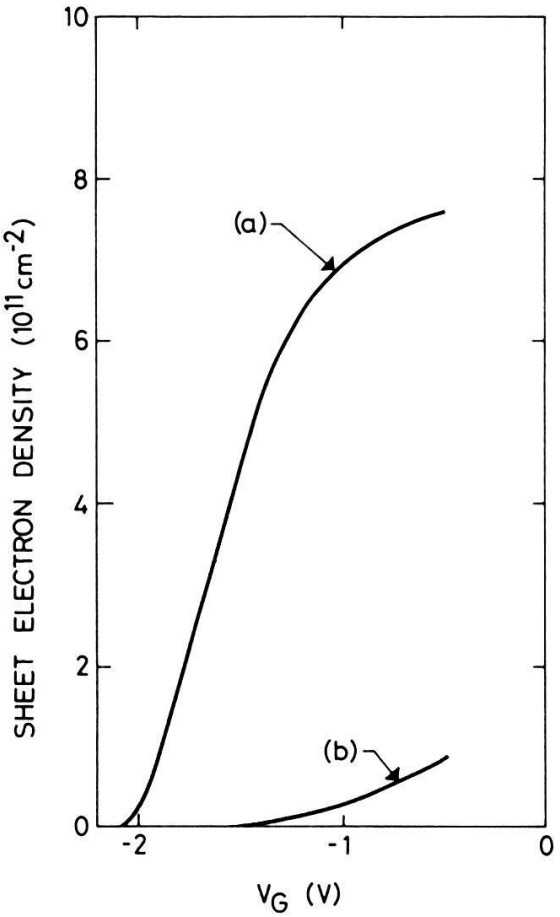

Figure 4
Calculated self-consistent electron density (a) in the channel and (b) in the AlGaAs layer as a function of gate voltage for the device of Fig. 3. At 300 K, 60% and 20% of the electrons are located in the first and second subband, respectively (after Vinter [14]).

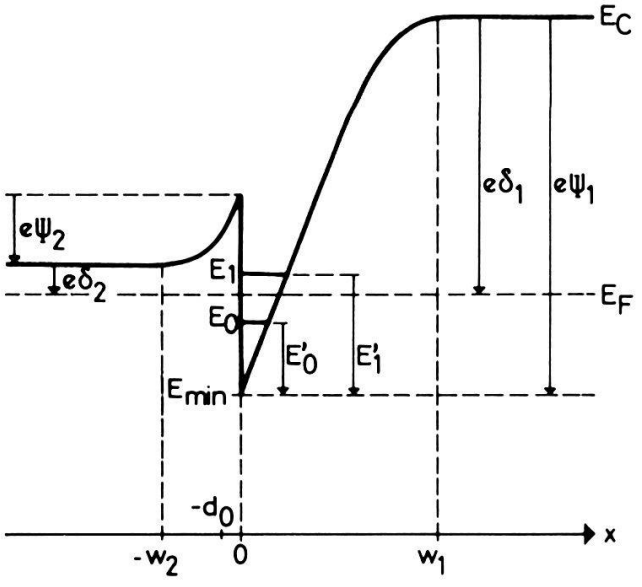

Figure 5
Schematic illustration of the conduction band edge across a AlGaAs/GaAs heterojunction showing quantities that enter in equations (9) to (22). E_0 and E_1 designate the energies of the lowest subband edges and E'_0 and E'_1 the distance from the subband edge to the potential well minimum

(b) *Triangular well model with depletion approximation*

This approach takes as starting hypothesis that the electric field $\mathscr{E}$ in the potential well is constant (triangular well approximation) and equal to its value $\mathscr{E}_{i1}$ at the interface on the GaAs side. In that case, the subband energies $E_0', E_1', \ldots$ measured from the bottom of the well $E_{\min}$ (see Fig. 5) are given by

$$E_n' = (\hbar^2/2m_n)^{1/3}(3\pi e\mathscr{E}_{i1}/2)^{2/3}(n+3/4)^{2/3} = \gamma_n \cdot \mathscr{E}_{i1}^{2/3} \tag{9}$$

where the γ_n's are numerical constants.

The electric fields at the interface, $\mathscr{E}_{i1}$ and $\mathscr{E}_{i2}$ on the GaAs and AlGaAs sides, respectively, are determined by solution of the Poisson's equation. One has, on the low bandgap GaAs side ($x \geqslant 0$), depending on whether the material is residually doped p- or n-type:

$$d\mathscr{E}/dx = -(e/\varepsilon_1)[n(x) + N_{A1}^-] \quad (p\text{-type GaAs}) \tag{10a}$$

or

$$d\mathscr{E}/dx = -(e/\varepsilon_1)[n(x) - N_{D1}^+] \quad (n\text{-type GaAs}) \tag{10b}$$

where $n(x)$ is the free electron concentration and N_{A1} or N_{D1} the ionized residual acceptor or donor concentration. Using the depletion approximation one finds, after integrating over a space charge width w_1 and assuming that the material is neutral for $x \geqslant w_1$

$$\mathscr{E}_{i1} = (en_s + eN_{A1}w_1)/\varepsilon_1 \quad (p\text{-type GaAs}) \tag{11a}$$

$$\mathscr{E}_{i1} = (en_s - eN_{D1}w_1)/\varepsilon_1 \quad (n\text{-type GaAs}) \tag{11b}$$

where n_s is the 2D-electron density. In order to achieve high mobilities in the channel, the GaAs doping is held as low as possible and the contribution from the fixed charges in equation (11) is generally negligible before the en_s term so that, to a good approximation

$$\mathscr{E}_{i1} = en_s/\varepsilon_1 \tag{12}$$

irrespective of residual GaAs layer doping.

Similarly one finds, for Poisson's equation on the high bandgap n-type AlGaAs side ($x \leqslant 0$)

$$d\mathscr{E}/dx = -(e/\varepsilon_2)[n(x) - N_{D2}^+(x)] \tag{13}$$

where N_{D2} is the AlGaAs doping density. Upon integrating over the width of a space charge region w_2 (see Fig. 5), neglecting the concentration of mobile carriers, and taking into account the presence of a nominally undoped spacer layer of width d_0, one finds as before

$$\mathscr{E}_{i2} = eN_{D2}(w_2 - d_0)/\varepsilon_2 \tag{14}$$

The width of the space charge region w_2 is related to the total amount of band bending ψ_2 on the AlGaAs side by

$$\psi_2 = (eN_{D2}/2\varepsilon_2)(w_2^2 - d_0^2) \tag{15}$$

Upon substituting for w_2 in equation (14), one finds finally

$$\mathscr{E}_{i2} = +\sqrt{2e\varepsilon_2 N_{D2}\psi_2 + e^2 N_{D2}^2 d_0^2}/\varepsilon_2 - eN_{D2}d_0/\varepsilon_2 \tag{16}$$

Neglecting interface charges, one has the continuity condition for the displacement vector

$$\varepsilon_1 \mathscr{E}_{i1} = \varepsilon_2 \mathscr{E}_{i2} \tag{17}$$

and hence the relation for the sheet density

$$n_s = \sqrt{2\varepsilon_2 N_{D2}\psi_2/e + N_{D2}^2 d_0^2} - N_{D2} d_0 \tag{18}$$

The sheet electron density n_s and the band bendings ψ_2 and ψ_1 in AlGaAs and GaAs can be expressed in terms of the relative positions of the potential well minimum E_{min} with respect to the Fermi level E_F. For the equilibrium case (no gate voltage) one has, from Fig. 5,

$$\psi_2 = \Delta E_c/e - \delta_2 - (E_F - E_{min})/e \tag{19}$$

where δ_2 is determined by the doping level in AlGaAs. Hence, upon substitution of equation (19) in (18) one obtains

$$n_s = \sqrt{2\varepsilon_2 N_{D2}(\Delta E_c/e - \delta_2 - E_F + E_{min})/e + N_{D2}^2 d_0^2} - N_{D2} d_0 \tag{20}$$

The sheet electron density, on the other hand, is given by the sum of the occupancies of the different subbands. According to equations (5) to (7), by integrating over the full well width in each band:

$$\begin{aligned} n_s &= D \sum_n N_n \\ &= kTD \sum_n \ln [1 + \exp (E_F - E_n)/kT] \end{aligned} \tag{21}$$

In equation (21), values of E_n depend on the total electron concentration n_s. With the triangular well approximation one has, following equations (9) and (12)

$$E_n = E_{min} + E_n' = E_{min} + \gamma_n \cdot \mathscr{E}_{i1}^{2/3} = E_{min} + \gamma_n (e n_s/\varepsilon_1)^{2/3} \tag{22}$$

The set of equations (20–22) can be solved iteratively by starting with a trial value for $(E_F - E_{min})$ and continuing until equations (20) and (21) give identical results. The results of the iterative calculation are plotted in Fig. 6 from Ref. 15 as n_s versus N_{D2} for different values of the spacer width d_0.

In the TEGFET case, where the AlGaAs layer is contacted by a Schottky gate, the above analysis must be modified. In normal operation, the AlGaAs layer is fully depleted to prevent parallel conduction paths. We have in this case for the total band bending (Fig. 7), by integrating over the interface sheet charge en_s and the fixed charge density eN_{D2} from $x = -d_2$ to $x = 0$:

$$\psi_2 = e n_s d_2/\varepsilon_2 - e N_{D2}(d_2 - d_0)^2/2\varepsilon_s \tag{23}$$

The band bending is related to the applied gate voltage V_G by (see Fig. 7)

$$\psi_2 = \phi_{ms} + V_G - \Delta E_c/e + (E_F - E_{min})/e \tag{24}$$

Then finally, by solving for n_s between equations (23) and (24)

$$n_s = (\varepsilon_2/e d_2)[\phi_{ms} + V_G - (\Delta E_c - E_F + E_{min})/e] + N_{D2}(d_2 - d_0)^2/2d_2 \tag{25}$$

In general, the $(E_F - E_{min})$ term on the right hand side is small compared to the ΔE_c or $e\phi_{ms}$ terms and may be neglected. With this assumption, one defines a

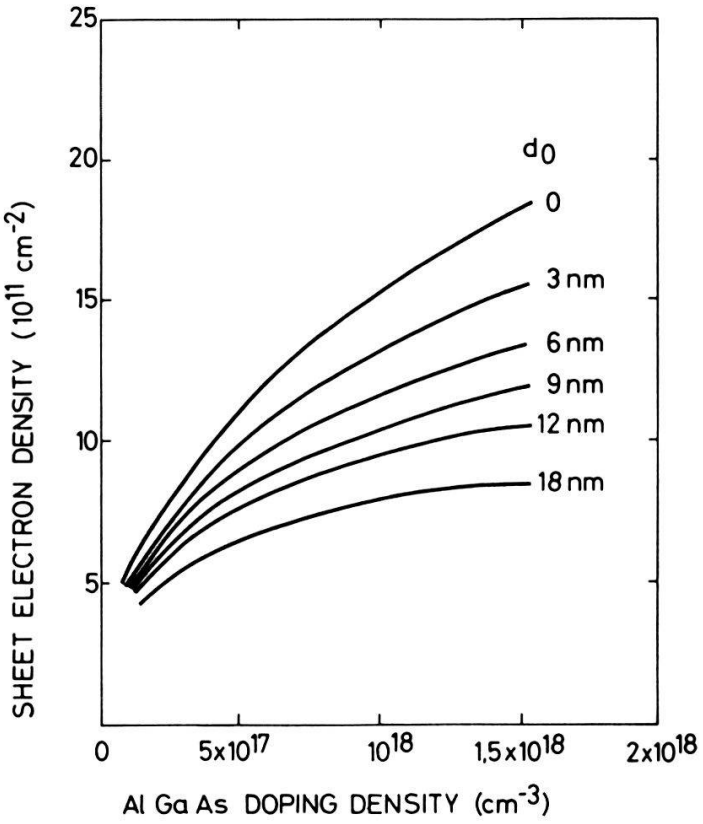

Figure 6
Sheet electron concentration n_s of the two-dimensional electron gas as a function of AlGaAs dopant concentration N_{D2} and spacer thickness d_0. (after Delagebeaudeuf and Linh [15]).

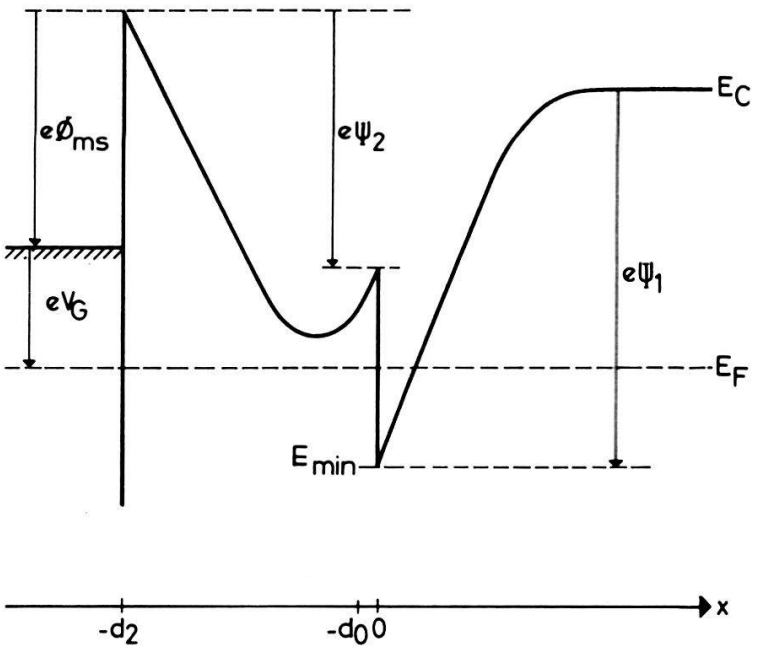

Figure 7
Schematic diagram of the conduction band edge across a AlGaAs/GaAs heterojunction with Schottky gate contact, showing quantities that enter in equations (23) to (27).

gate off-voltage, $V_{G,off}$, which annihilates the $2D$-gas ($n_s = 0$), i.e.

$$-V_{G,off} = \phi_{ms} - \Delta E_c/e + eN_{D2}(d_2 - d_0)^2/2\varepsilon_s \tag{26}$$

Using this definition and neglecting again the $(E_F - E_{min})$ terms, equation (25) can be rewritten in the form

$$n_s = (\varepsilon_2/ed_2)(V_G - V_{G,off}) \tag{27}$$

which is formally identical to the corresponding equation for the inversion layer density in a silicon MOSFET transistor. A comparison between this result and the nearly exact calculation exemplified by Fig. 4 shows that the linear relationship predicted by equation (27) holds over a large portion of the n_s versus V_G characteristics.

From this point on, the analysis for the TEGFET transistor proceeds in a similar manner as that for a Si MOSFET. In particular, the expression for the current at a given point y along the channel direction is

$$I_D = e \cdot n_s(y) \cdot v(y) \cdot W \tag{28}$$

where $n_s(y)$ is the interface charge density at y, W the gate width, and $v(y)$ the electron velocity at y which depends in a complex manner on the different scattering mechanisms present (phonon scattering, intervalley scattering, electron–electron scattering, intrasubband scattering, real space transfer scattering, etc.) as will be discussed further below.

3. Low-field mobility of 2*D*-electron gas

Mobilities in bulk GaAs are primarily limited by polar optical (*PO*) phonon scattering at high temperatures and by ionized impurity (*I*) and acoustic (*A*) phonon scattering at low temperatures. The temperature dependence of these different mechanisms is illustrated schematically in Fig. 8 for a layer with a background doping level of $N_I = 1 \times 10^{15}\,\text{cm}^{-3}$, where N_I represents the total concentration of ionized impurities present. The maximum mobilities reported [19, 20] for extremely high purity bulk layers grown by vapor phase or liquid phase epitaxy are in the range from 2×10^5 to $2.5 \times 10^5\,\text{cm}^2/\text{Vs}$ at ~ 50 K, close to the theoretical limit, and decrease to values around 1×10^4 to $4 \times 10^4\,\text{cm}^2/\text{Vs}$ at $T \sim 10$ K because of the increased influence of ionized impurity scattering.

In $2D$ systems with the same level of ionized impurity concentrations, much higher low temperature mobilities can be achieved because of the effective screening of the Coulomb attractive impurity centers by the high density electron gas. The resulting behavior is illustrated in Fig. 9, where we show mobility versus temperature data for a thick ($\sim 4\,\mu$m) and $2D$-selectively doped GaAs layer grown in the same system, characterized by a (relatively high) background residual impurity level around $2 \times 10^{15}\,\text{cm}^{-3}$.

Theoretical model calculations by Stern [17] indicate that the scattering by residual ionized impurities in the $2D$-channel remains the dominant limiting factor in selectively doped heterointerface devices. Assuming that the background acceptor doping level in the undoped GaAs and AlGaAs spacer layer can be held down to $1 \times 10^{14}\,\text{cm}^{-3}$, a peak mobility of $\mu_{max} = 2.2 \times 10^6\,\text{cm}^2/\text{Vs}$ is calculated at a sheet electron density around $n_s = 1.3 \times 10^{11}\,\text{cm}^{-2}$. An increase in the back-

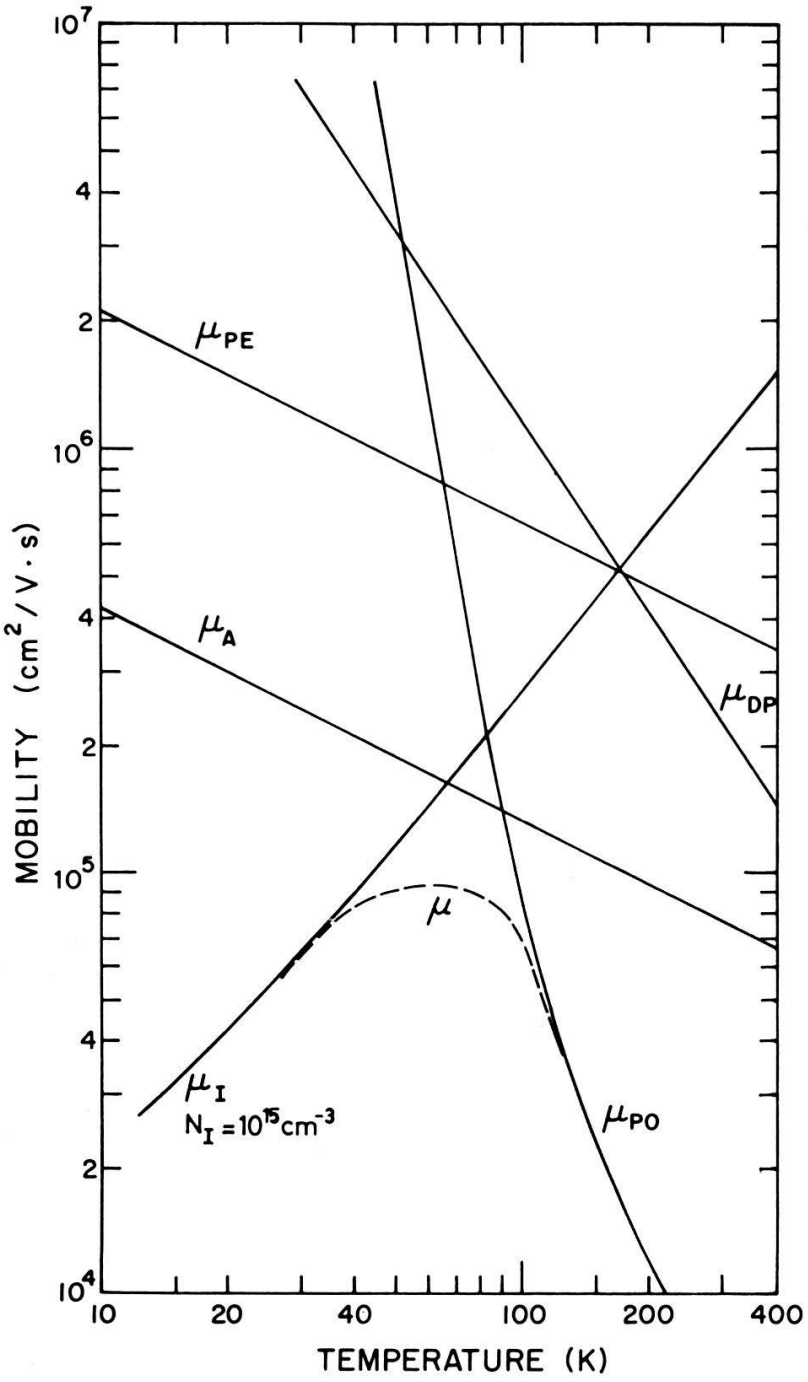

Figure 8
Schematic illustration of the influence of the different scattering mechanisms in limiting the overall mobility (dashed curve) in high purity ($N_I \sim 1\times10^{15}\,\mathrm{cm}^{-3}$) bulk GaAs.

ground doping level from 1 to $3\times10^{14}\,\mathrm{cm}^{-3}$ reduces the peak mobility to $9\times10^{5}\,\mathrm{cm}^2/\mathrm{Vs}$ at $n_s = 1.7\times10^{11}\,\mathrm{cm}^{-2}$. In addition to channel and spacer ionized impurity scattering, Coulomb scattering from the space charge layer in the doped AlGaAs, interface roughness scattering, and alloy scattering in AlGaAs contribute to limiting the overall peak mobility [21–23].

Mobilities are expected to improve with increased separation of the mobile carriers from the strongly scattering ionized impurities in AlGaAs. Theoretically, the optimum strategy would be to use the maximum spacer layer thickness d_0 compatible with the desired channel density n_s; this maximum spacer thickness

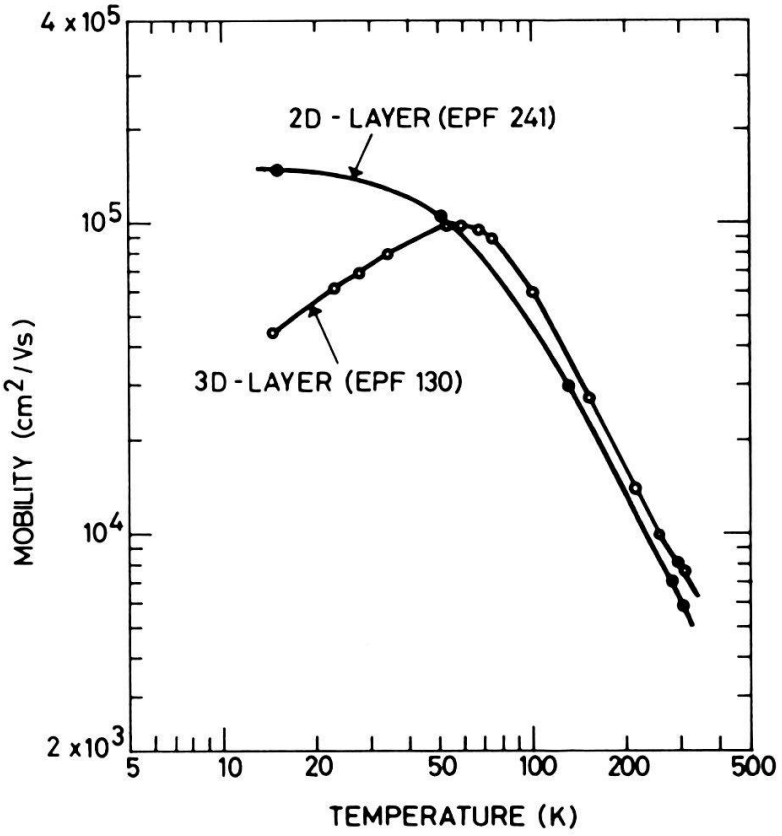

Figure 9
Electron mobility versus temperature measured for (a) a Si-doped 6 μm thick epitaxial layer and (b) a 2D-electron gas at a selectively doped interface grown in the same system. Mobilities are relatively low because of a high concentration of background impurities ($N_I \sim 2\times 10^{15}\,\mathrm{cm}^{-3}$) present in the system.

will thus be determined by the highest doping densities that can be achieved in AlGaAs and depends on the solubility limit of the particular donor used. In practice, because the reproducible control of the level of residual impurities is difficult, the predicted behavior is not always experimentally verified, and very high mobilities [11, 12], nearly uncorrelated with d_0, have been achieved in structures with spacer width between ~6 and ~40 nm.

In the highest purity growth systems, low-field mobilities of $\sim 1\times 10^6\,\mathrm{cm}^2/\mathrm{Vs}$ in the dark [10, 12] and of 1.6×10^6 to $2.1\times 10^6\,\mathrm{cm}^2/\mathrm{Vs}$ after illumination with the layer in the persistent photoconductive mode [24] have been reported. These peak mobilities occur at channel densities around $2.2\times 10^{11}\,\mathrm{cm}^{-2}$ (dark values) and 3.6 to $3.9\times 10^{11}\,\mathrm{cm}^{-2}$ (under illumination). These areal densities are equivalent to a bulk carrier concentration around $2\times 10^{17}\,\mathrm{cm}^{-3}$, where the corresponding low temperature mobility would be significantly below $10^4\,\mathrm{cm}^2/\mathrm{Vs}$; this indicates that the mobility of the $2D$-gas can exceed that of equivalently doped bulk material by more than 2 orders of magnitude.

The temperature dependence of the mobility in a high quality $2D$ layer which exhibits a peak mobility $\sim 1.6\times 10^6\,\mathrm{cm}^2/\mathrm{Vs}$ after illumination is shown in Fig. 10, together with theoretical curves [22] (solid line) calculated assuming Matthiessen's rule. The calculation takes into account ionized impurity scattering due to residual background doping in the channel and spacer layer (μ_{BI}), ionized impurity scattering due to the remote donors in the space charge layer (μ_{RI}), polar optical

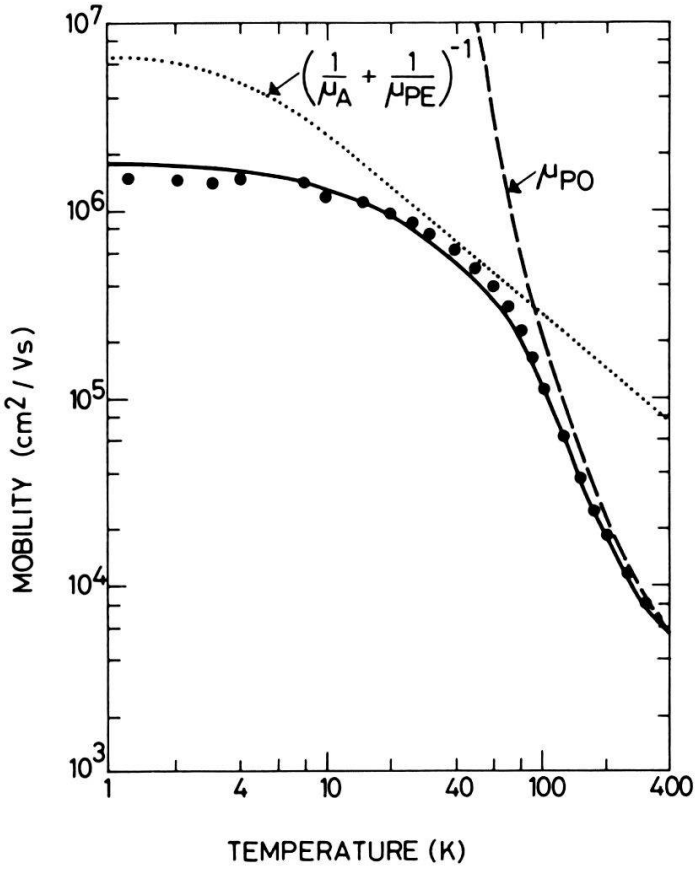

Figure 10
Temperature dependence of the mobility in a high quality $2D$-layer, compared to theoretical curves calculated assuming Matthiessen's rule (after Lee et al. [22]).

(μ_{PO}), acoustic (μ_A) and piezoelectric (μ_{PE}) scattering mechanisms, with the overall mobility given by

$$1/\mu = 1/\mu_{BI} + 1/\mu_{RI} + 1/\mu_{PO} + 1/\mu_A + 1/\mu_{PE} \tag{29}$$

A good agreement with the data is achieved by fitting the curve using a temperature-independent value of $2.5\times10^6\,cm^2/Vs$ for the $(1/\mu_{BI} + 1/\mu_{RI})$ Coulomb scattering terms. Studies of the temperature dependence of the electron mobility indicate that the low temperature mobility in these $2D$-systems will ultimately be limited by acoustic deformation potential scattering [23]. Theoretical predictions [22] based on fitted values for acoustic and piezoelectric scattering put the maximum mobility limit near $6.5\times10^6\,cm^2/Vs$ for $n_s \sim 4\times10^{11}\,cm^{-2}$.

4. Field effect transistor applications

(a) *Carrier velocity considerations*

Because of the high velocity with which the electrons can travel through the $2D$-layer, these selectively doped interface structures are of interest for fast logic switching or high frequency amplification applications. Switching speeds of active semiconductor devices are determined by how fast an input pulse can be transmitted to the output, and depend on the intrinsic transit time and on the charging

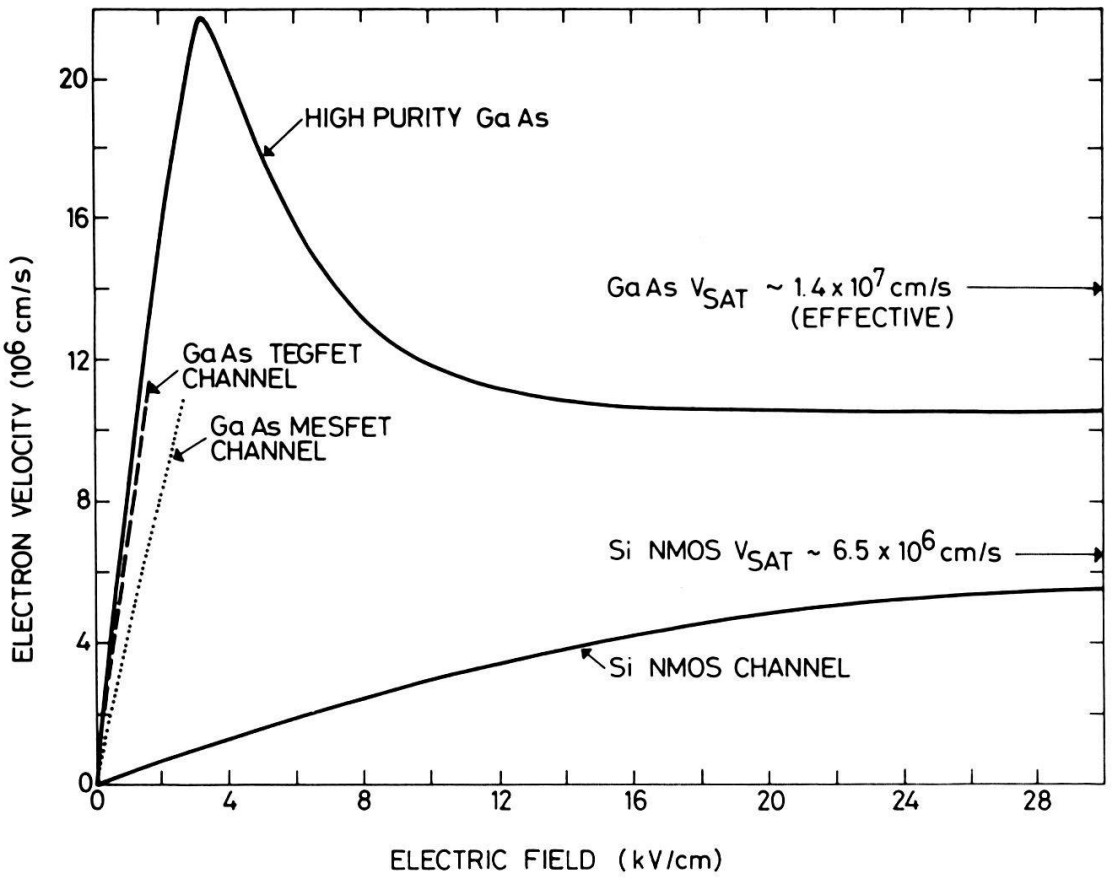

Figure 11
Equilibrium velocity-field characteristics for electrons in (a) high purity bulk GaAs, (b) a GaAs TEGFET channel with $n_s \sim 7 \times 10^{11}\,\text{cm}^{-2}$, (c) a GaAs MESFET channel with $N_D = 2 \times 10^{17}\,\text{cm}^{-3}$ doping level, and (d) a MOSFET channel with $n_s \sim 7 \times 10^{12}\,\text{cm}^{-2}$. The effective GaAs saturation velocity applies to 1 μm channel MESFET devices. (after Eden [25]). Data for 300 K.

time of the input and output capacitances of the device and its associated wiring. Capacitance charging times depend on the circuit design and minimum geometries used, as well as on the amount of current available. Transit times similarly depend on the current path length and on the speed of carriers.

Electron transport in TEGFET's is dominated by high field effects [25, 26]. Because of the short gate lengths used (typically ≤ 1 μm), the longitudinal electric field components are quite large ($\mathscr{E} \geq 10^4$ V/cm) even at moderate source to drain voltages and carrier velocities reach their limiting values (Fig. 11). Effective saturation velocities encountered in short channel devices are higher than the equilibrium values given by the solid curve because transit times are too short to allow complete electron transfer to the higher conduction band minima to take place. These 'velocity overshoot' or 'ballistic' effects lead to improvements in speed performance as the gate lengths and/or the operating voltages are reduced [25].

Because in the selectively doped TEGFET the speed of carriers is not limited by ionized impurity scattering, both its low field and saturating velocity limits are higher than those found in a conventional MESFET, especially at 77 K temperatures and below. As a guideline rule, one finds that the transport behavior of transfer doped TEGFET's with a channel density n_s around $7 \times 10^{11}\,\text{cm}^{-2}$ are comparable to those of pure undoped bulk GaAs; in particular, electron peak

velocities of 2×10^7 cm/s at 300 K and 3×10^7 cm/s at 77 K may be obtained [26]. In corresponding GaAs MESFET's of equivalent bulk doping level around 10^{17} cm^{-3}, these values are reduced because of the large concentration of dopants atoms present. As a result, TEGFET structures should permit a speed improvement of ~20% at 300 K and ~60% at 77 K over conventional MESFET's [26].

(b) *TEGFET transconductance*

The operation of the GaAs/AlGaAs TEGFET is in principle similar to that of the Si/SiO_2 MOSFET, the depleted AlGaAs layer playing the role of the SiO_2 insulator. As for the MOSFET, two types of devices can be distinguished. In *depletion-mode* devices, of the type illustrated in Fig. 3, the depletion by the gate built-in potential is just sufficient to have the surface depletion extend into the interface depletion region. Without applied gate voltage, the channel will be populated with $\sim5\times10^{11}$ to 1×10^{12} electrons/cm^2 coming from the interface depletion region; a ~1 to ~2 V negative gate bias is required to turn the device off. In *enhancement-mode* devices, the thickness or doping level of the AlGaAs under the gate is lower and the depletion region under the Schottky barrier extends through the AlGaAs and depletes the 2*D* interface well. No current flows until a positive bias is applied to the gate. Because of power dissipation considerations, enhancement-mode TEGFET's are used as active transistor switches in digital integrated circuits, while depletion-mode devices with the gate shortened to the source or ungated saturated resistors are used as loads.

Away from the cutoff regime, the capacitance under the gate is nearly constant and the channel electron density n_s is proportional to the gate voltage minus the threshold voltage as given by equation (27). At voltages close to the gate off-voltage $V_{G,\text{off}}$, n_s versus V_G deviates from a linear behavior as shown previously in Fig. 4. The region of curvature at low n_s may extend over 0.1 to 0.2 V, which sets a minimum limit to the circuit voltage of ~0.5 to 1 V for high speed operation.

The transconductance of the TEGFET in the saturation regime, neglecting limiting velocity effects, is given to first order by the well known relation derived originally for MOSFET's

$$g_{m,\text{sat}} = \partial I_D/\partial V_G = (\varepsilon_2\mu_n W/d_2 L)(V_G - V_{G,\text{off}}) \tag{30}$$

where μ_n represents the average electron mobility, W and L the device width and length, respectively, d_2 the gate to channel distance, and ε_2 the AlGaAs dielectric constant. Because of the higher mobilities, higher dielectric constant, and very narrow AlGaAs layer width (typically 40 nm), the transconductance should be larger for the GaAs TEGFET than for a Si MOSFET of equivalent geometries. In addition, because of the excellent quality of the AlGaAs/GaAs interface, the density of interface states in the TEGFET structure is reduced below that of a MOSFET device. As a disadvantage, one should refer to the limited allowable gate voltage before condition in the AlGaAs becomes important, and to the lower gate input resistance as determined by the reverse leakage currents of the Schottky barrier gate.

In reality, electrons travel through the TEGFET channel with velocities close to their limiting value. The maximum saturation current from the 2*D*-layer is then

given simply by

$$I_{D,\max} = en_s v_{sat} W \tag{31}$$

and, taking into account the nearly linear relation between n_s and V_G given by equation (27), the expression for the transconductance reduces to

$$g_{m,sat} = \varepsilon_2 v_{sat} W/d_2 \tag{32}$$

independent of gate length neglecting ballistic effects. An upper limit for the current gain-bandwidth product in this regime is given by

$$f_T \sim g_m/2\pi C_g \sim v_{sat}/2\pi L_g \tag{33}$$

where C_g is the device output capacitance assumed equal to the gate capacitance.

Maximum transconductances reported to date for TEGFET devices with 1 μm gate length are around 270 mS/mm gate width at 300 K and 400 mS/mm gate width at 77 K [26, 27]. These results should be compared to optimum values around 230 mS/mm for GaAs MESFET [25], 180 mS/mm for 0.15 μm channel Si MOSFET [28], and 80 mS/mm for 1 μm channel Si MOSFET devices. In addition to the advantages of a higher transconductance, the TEGFET drain current versus gate voltage characteristics exhibit a sharper turn-on than is the case for MESFET or MOSFET devices (Fig. 12). This sharp turn-on maximizes the load current for a given voltage swing and hence results in greater logic switching speed.

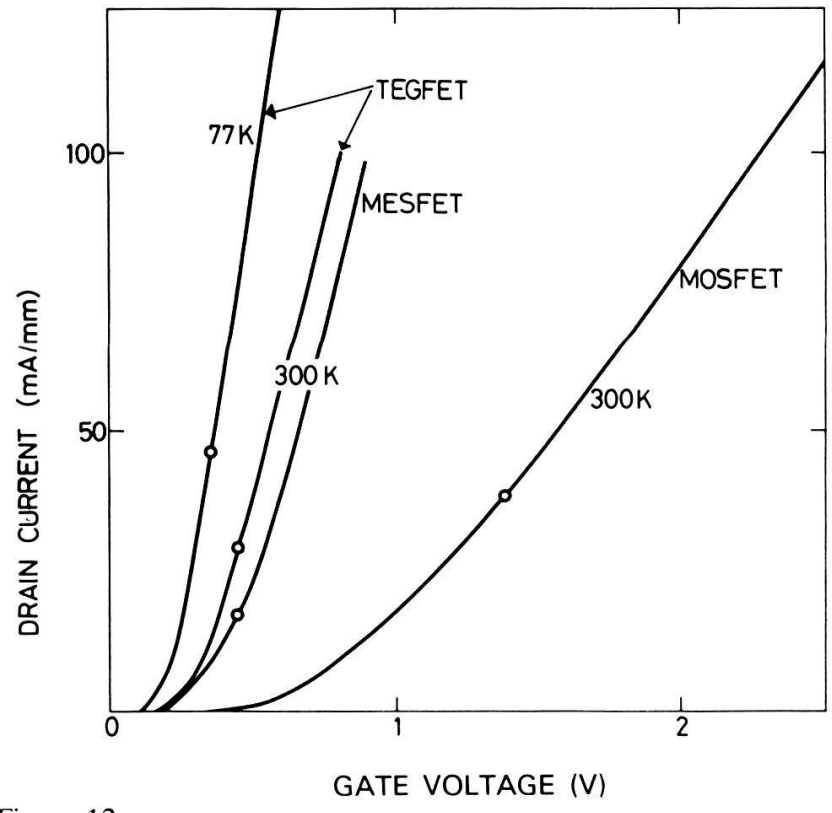

Figure 12
Comparison of saturated current versus gate voltage characteristics for a GaAs TEGFET, GaAs MESFET, and Si MOSFET transistor. Curves are for 1 μm gate length devices and are shifted along the voltage axis for comparison purposes. (after Solomon and Morkoç [26]).

(c) *Switching speeds*

A number of laboratories have reported on switching speeds measured in ring oscillator or frequency divider test circuits using TEGFET transistors [4–7, 29–32]. The best results reported to date for circuits developed with a 1 μm gate technology are in the range from 9.8 ps [29] to 12.8 ps [30] per gate at 77 K and from 12.2 ps [6] to 18.4 ps [31] per gate at 300 K. These high switching speeds are obtained at relatively low power dissipation per stage (typically $\leq$1 mW/gate), resulting in very low power-delay product, the optimum value reported being ~4 fJ per stage at a switching speed of 27 ps [32]. The low power dissipation achieved indicates that high levels of integration ($\geq 10^5$ gates/chip) can be envisioned. This latter property is an important factor when considering high speed digital system applications, since it is clear that, because of the increasing importance of interchip and package delays, GaAs will only be able to compete successfully with other technologies when very high levels of integration can be achieved.

The experimental results quoted above are close to the values obtained from first order theoretical estimates. Taking as an example a typical enhancement mode inverter TEGFET device with $L_g = 0.5$ μm for the gate length, $W = 50$ μm for the gate width, $C_p = 10$ fF for the output capacitance, operated with a ~1 V power supply and a ~2.5 mA peak current, one finds,
– for the delay time

$$\tau_d \sim L_g/v_{sat} + C_p V/I \sim 8 \text{ ps}$$

– for the power-delay product

$$P \cdot \tau_d \sim \tfrac{1}{2} IVL_g/v_{sat} + \tfrac{1}{2} C_p V^2 \sim 10 \text{ fJ}$$

These estimates also clearly illustrate the trade-off between power and speed, as well as the influence of gate length and parasitic circuit capacitances.

The advantages of high speed and low power are enhanced by low temperature (77 K) operation, and are likely to form the basis for the application of TEGFET devices in future supercomputer systems. The low temperature operation leads to improvements in switching speed (because of the ~50% larger peak and saturation velocity values) and in a reduction of the power-delay product since lower supply voltages can be used (sharper turn-on). In addition, there are important improvements in other areas such as better conductivity of metal interconnexion lines, improved GaAs thermal conduction, elimination of electromigration effects at high current levels, and much enhanced retention times for dynamic memory circuits.

(d) *Comparison with other technologies*

Comparisons with other technologies are always difficult, especially since the device performance can often not be separated from the circuit aspects. To date, the best 300 K figures available for n-channel Si MOSFET's with 0.3 μm gate length are 28 ps/gate delay time and 40 fJ/stage power-delay product in a ring oscillator configuration [33]. Complementary Si MOSFET's circuits are capable of much lower power-delay products with however a longer delay per stage. The

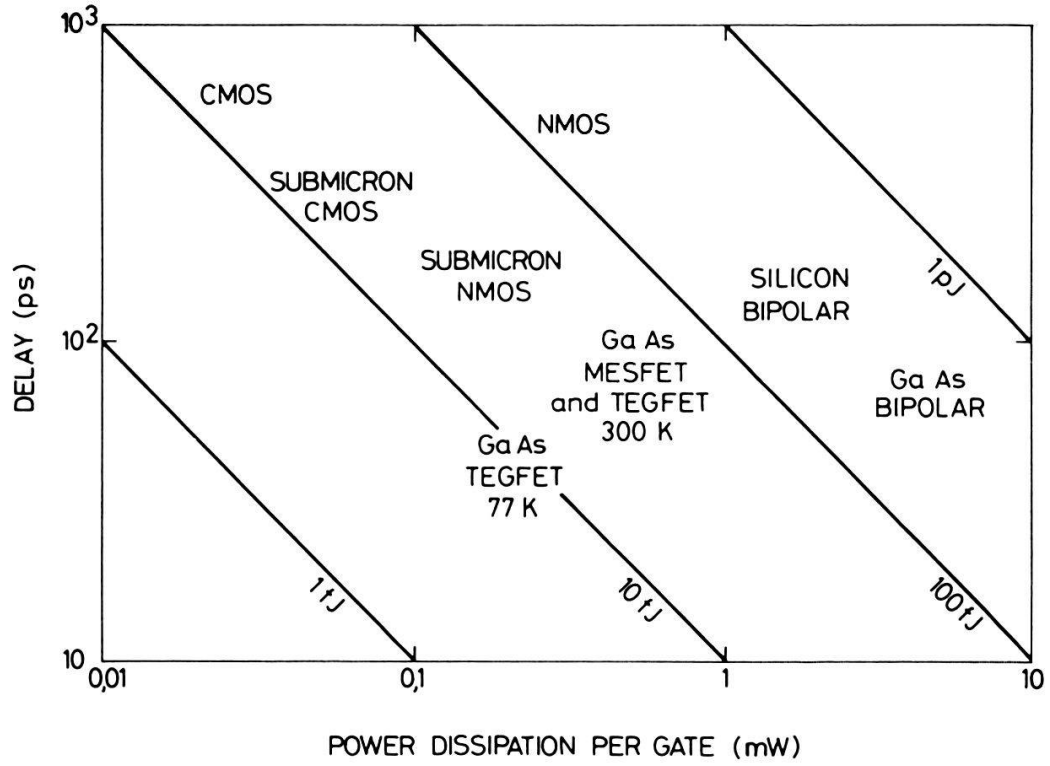

Figure 13
Predicted switching delay versus power dissipation per gate for different logic circuit technologies. Diagonals are lines of constant power-delay product. (after Solomon and Morkoç [26]).

performance of the Si based circuits is expected to continue to improve as technology advances, and could be further enhanced by going to low temperature operation.

A comparison summary of expected delay versus performance behavior for various semiconductor technologies in a large scale integrated circuit environment is shown in Fig. 13 from Ref. 26. It is clear that the advantages of GaAs MESFET and TEGFET circuits lie inherently in the high speed area presently dominated by the Si bipolar transistor. At 300 K, short gate MESFET and TEGFET performance predictions are similar, but the TEGFET would show a clear advantage at 77 K operation. Finally the trade-off between a 77 K GaAs TEGFET and a 300 K or 77 K submicron Si CMOS technology is one of speed versus power, the TEGFET retaining a clear advantage when ultrafast operation is essential.

5. Conclusions

The field concerned with the development of GaAs devices and circuits is one of intense activity, with new approaches constantly being explored and evaluated against a rapidly advancing Silicon performance standard. Despite the many obstacles that remain, the selectively doped TEGFET approach shows great promise for large scale ultrafast digital circuit and low-noise high-frequency analog applications. In addition, the study of these devices has revealed new detailed aspects of semiconductor device physics and has formed the basis for

exciting experiments dealing with the quantized transport in $2D$ electron gas systems at low temperatures and high magnetic fields.

Outside optoelectronic and microwave applications, the real impact of the GaAs technology should be in the area of very large scale logic circuits. At present, 16 kbit static memories with $>10^5$ transistors per chip are in industrial development [34] based on a self-aligned ion implant MESFET technology. A sustained effort will be necessary to bring the TEGFET approach to the same level, the main problems being those of substrate quality, epitaxial layer morphology and growth defects, control of materials doping and residual deep level trap concentration, threshold voltage uniformity and contact metallurgy. The solution of these difficult materials problems represents an important challenge for future work in the field, and should prepare the way for the development of an industrially viable VLSI TEGFET technology.

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