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Elektrotechnik – Electrotechnique

Moderne Technologien in der Elektronik

Über dieses Thema führte der SEV am 11. November 1976 in Biel eine gut besuchte Informationstagung durch. Wir veröffentlichen nachfolgend die fünf Vorträge in leicht gekürzter Form. Auf Seite 70 befindet sich zudem eine Tabelle mit der Bedeutung der verwendeten Abkürzungen.

Integrated Injection Logic

By J. Lohstroh

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I^2L fulfils the most stringent boundary conditions for LSI: high packing density and low power consumption. Analog, TTL and I^2L circuitry can be combined on the same chip using existing bipolar technologies. For speeds up to 50 ns the existing technologies can be used; for higher speeds up to 3...5 ns new generation technologies have to be introduced. In this article both an introduction and a survey of the state of the art of I^2L is given.

I^2L erfüllt die härtesten an LSI gestellten Randbedingungen: hohe Packungsdichte und niedriger Leistungsbedarf. TTL und I^2L-Schaltungen können zudem auf demselben Plättchen mittels bekannter bipolarer Technologie kombiniert werden. Für Geschwindigkeiten bis 50 ns sind bekannte Technologien verwendbar; für höhere Geschwindigkeiten bis 3...5 ns sind neue Technologien notwendig. Der Aufsatz gibt eine Einführung und einen Überblick über den Stand der Technik von I^2L.

I^2L remplit les conditions les plus strictes posées à la LSI: densité élevée et consommation de puissance faible. De plus, les circuits TTL et I^2L peuvent être combinés sur une seule puce au moyen des technologies bipolaires existantes. Pour une vitesse de 50 ns, les technologies existantes sont utilisables, pour des vitesses supérieures jusqu'à 3...5 ns de nouvelles technologies doivent être introduites. L'article présente une introduction et une vue d'ensemble sur l'état de la technique de la technologie I^2L.

1. Introduction

Since 1972, Integrated Injection Logic, I^2L, the new approach to bipolar LSI[1]) design, is catching the imagination of logic designers throughout the world. The new logic was simultaneously presented by two research laboratories at the International Solid State Circuits Conference in Philadelphia, USA [1; 2][2]). After four years of intensive research and preproduct development, the semiconductor industry is beginning to understand I^2L, and the first products are now available [3].

The succes-story of I^2L is easily explained. Namely the most stringent boundary conditions for LSI, good packing density and low power dissipation are fulfilled by this logic. Moreover I^2L can be made in existing bipolar processes, which means that every bipolar semiconductor house is able to produce it. Because of the existing process, I^2L can be easily combined with other types of logic and even analog circuits on the same chip.

Undoubtedly, for a four years old LSI approach, I^2L has made a dramatic impact. But the lingering question is whether I^2L will make it as a mainline digital technology in important areas such as microprocessors and memories where the main competitor, the metal oxide semiconductor (MOS)-LSI is already dominating. A mixture of costs, process availability, technical specifications, and second sourcing will influence the final outcome.

[1]) Large Scale Integration.
[2]) References are shown at the end of the paper.

2. Origin of the I^2L gate

Injection logic derives its layout from the old direct-coupled transistor logic (DCTL) structure shown in Fig. 1a [4; 5]. The circuit within the dashed lines consists of a number of transistors in parallel. Clearly, when one or more of them are ON they act as a short circuit, and no current is supplied to the load gates. Conversely, when they are all in the OFF state, current flows to the bases of the transistors in the load gates.

If the two transistors that have their bases connected are placed in a common region, the result is the circuit between the dashed lines in Fig. 1b. Next, the resistor in Fig. 1b is replaced by an active current source (to be described later), and transistors with connected bases are replaced by a multi-

collector transistor, an easy thing to do because all the DCTL transistors have a common emitter that is connected to ground. This basic I^2L configuration is presented in Fig. 1c.

The simple pnp-transistor shown in Fig. 1d can serve as the current source, by injecting minority carriers into the emitter region of the npn-transistor.

In any case, it is readily seen that the base of the npn transistor is common to the collector of the current source, while the base of the pnp-transistor is common to the emitter of the npn-transistor. The emitter of the pnp, common for all gates, is called the injector. On silicon, the entire gate takes up the space of a single multi-emitter transistor. Fig. 1d shows the the symbol of the I^2L gate and the symbol of the very well known nand gate (DCTL, TTL[3]), etc.). The I^2L gate has only one input and multiple outputs; the logic has to be made now in the wired logic technique.

To translate an original scheme with nand symbols to I^2L symbols is very simple. Every nand-gate has to be replaced by an I^2L gate with n collectors if a fan-out of n is used with the original nand-gate. The input of the I^2L gate is to be connected with the outputs of the gates which contributes to the fan-in of the corresponding nand. Further, different inputs of I^2L gates are not allowed to be interconnected. Fig. 2a shows a standard D-flip-flop built up with I^2L gates. As it is not allowed to interconnect the inputs of the I^2L gates 2 and 5 for the T node, an extra gate must be introduced with $\overline{T}$ at the input (Fig. 2b).

[3]) TTL = Transistor-Transistor Logic.
[4]) ECL = Emitter-Coupled Logic.

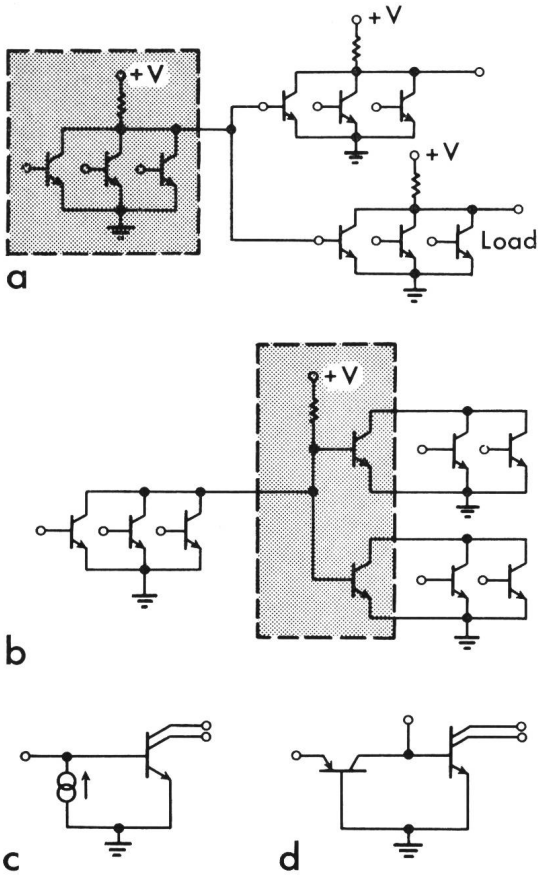

Fig. 1 Conversion of DCTL (a) into I^2L (d)
by placing the transistors with connected bases into a common region (b) and further replacing them by a multi-collector npn-transistor (c)

3. Building I^2L gates with a standard bipolar technology

Fig. 3 shows the cross-section of a typical circuit that combines I^2L gates with conventionally isolated transistors. Fabrication of the circuit starts with a p-type substrate containing discrete n^+-buried layers. The buried layer in the I^2L part of the circuit acts as a common emitter for the npn transistors and as a base for the pnp injector, while in conventional TTL or ECL[4]) logic it acts as collector for the isolated structures.

After the n-type epitaxial layer has been grown, a deep p^+-diffusion is performed to isolate the conventional components, while in the I^2L part the gates are isolated from each other by a deep n^+-diffusion. A p-type diffusion is then carried out to form all base regions and emitters of the lateral pnp transistors (the injectors of the I^2L gate). Next, a shallow n^+-diffusion forms both the collectors in the I^2L part of the circuit and the emitter and the collector contact regions for the conventional transistor structures. Two additional mask steps are needed for the contact holes and metallization. In all, only seven masks are required to manufacture both conventional isolated and I^2L transistors on the same chip. From this fabrication scheme it appears that I^2L can be combined on the same chip with any electronic circuit, analog or digital, which is made in the bipolar process.

4. Lay out and characteristics of the I^2L gate

Fig. 4 shows a cross section of an I^2L structure with two gates with the injector in the center. Each gate has two collectors and one contact to the base. The places of collectors and base contact can be interchanged in order to make simple lay-

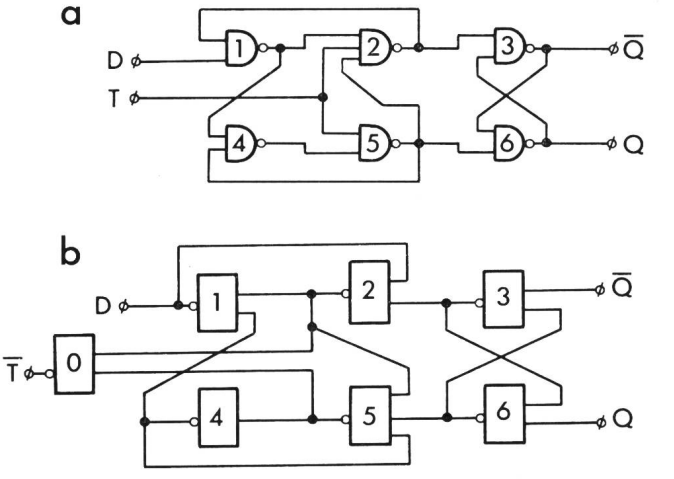

Fig. 2 (a) Standard D-flip-flop built up with nands (a) and (b) with I^2L gates (wired logic system)

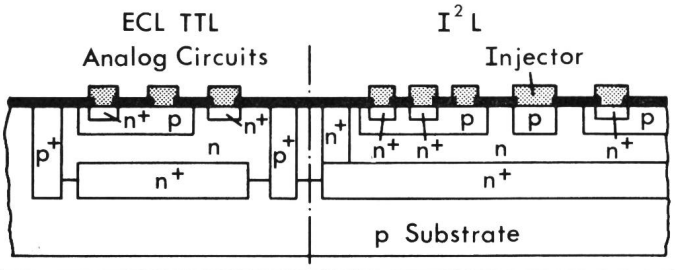

Fig. 3 Possibility of combining the bipolar I^2L technique with conventionally isolated transistors on one chip

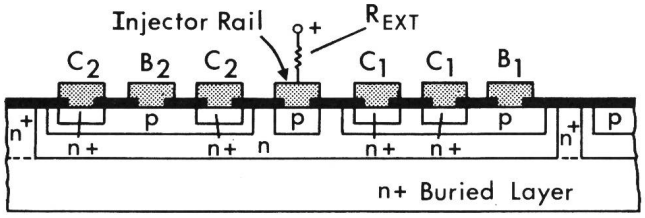

Fig. 4 Cross-section of an I²L structure with two gates with the injector in the center
The injector forms the emitter of the lateral pnp-transistor; holes are injected to both base areas of the multicollector npn-transistors. Heavily doped deep n+ isolation regions increase the current gain of the inverse operated npn-transistors and kill the parasitic effects of parasitic pnp-transistors between adjacent gates

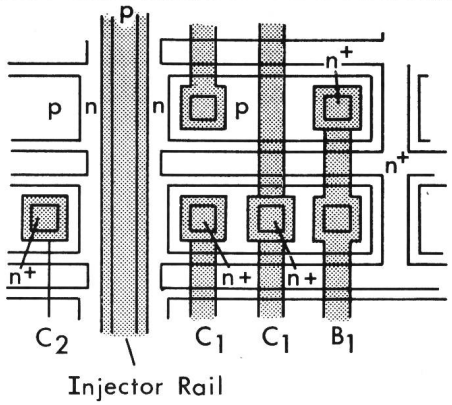

Fig. 5 Lay-out example
As the places of collectors and base contact can be interchanged, very simple lay-outs can be made

outs possible (Fig. 5). For regular circuits, e.g., shift registers, a packing density of 400 gates/mm² can be reached in a technology with 5 µm details; the packing density drops to about 250 gates/mm² for irregular structures [4].

The most characteristic fact in I²L is that the npn transistor is used in an inverse way. The low doped n-epilayer is the emitter and the high doped n⁺-diffusion at the top is the collector. This inverse mode of operation influences both the current amplification β_{up} and the cut-off frequency $f_{T\,up}$ of the transistor. In general β_{up} is much lower than β_{down} and also $f_{T\,up}$ is much lower than $f_{T\,down}$. Moreover β_{up} is affected by the presence of the merged pnp-transistor to which a back injection from npn base to pnp emitter takes place. If no recombination is assumed in the base of the pnp transistor it can be calculated [6] that

$$\beta_{up\,eff} = \frac{1}{\frac{I_{p0}}{I_{n0}} + \frac{1}{\beta_{up}}} \qquad (1)$$

in which I_{p0} and I_{n0} are the saturation currents of the pnp and npn transistors respectively and β_{up} the β of the inverse operated npn-transistor. In fact the $\beta_{up\,eff}$ is not allowed to be smaller than 2 or 3, in order to obtain a sufficient noise margin. With $\beta_{up} = 5$ and $I_{p0}/I_{n0} = 0.1$, $\beta_{up\,eff} \approx 3$.

Fig. 6 shows the $V_{in} - V_{out}$ characteristic of an I²L inverter. It can be calculated [6] that the voltage noise margin equals

$$\Delta V = \frac{kT}{q} \ln \beta_{up\,eff} \qquad (2)$$

With $\beta_{up\,eff} = 3$, ΔV will be about 27 mV. If $\beta_{up\,eff}$ becomes lower than one, the noise margin becomes negative, which means that the gate is useless. Therefore $\beta_{up\,eff}$ must be > 1.

Fig. 7 shows a curve representing measured propagation delay times versus power dissipation. This result was obtained from a five-stage closed-loop inverter chain with one collector for each inverter. The measured speed-power product was 1 pJ/gate for dissipation levels between 1 nW and 7 µW per gate. In the curve three dissipation levels are to be distinguished.

At low dissipation levels, i.e., between 1 nW and 1 µW, the propagation delay time is determined by junction and parasitic capacitances. The propagation delay time τ will be proportional to the time needed to charge and discharge these capacitances. As $Q = CV$ and $t = Q/I$, τ will be proportional to CV/I. The dissipation D will be $D = VI$, where V is the logic voltage swing. This logic voltage swing is almost equal to the voltage measured across the forward-biased junction of the injector. From this it follows that the speed-power product τD is proportional to CV^2, which is constant.

At medium dissipation levels, i.e., between 1 µW and 1 mW, the main influence on the propagation delay time comes from

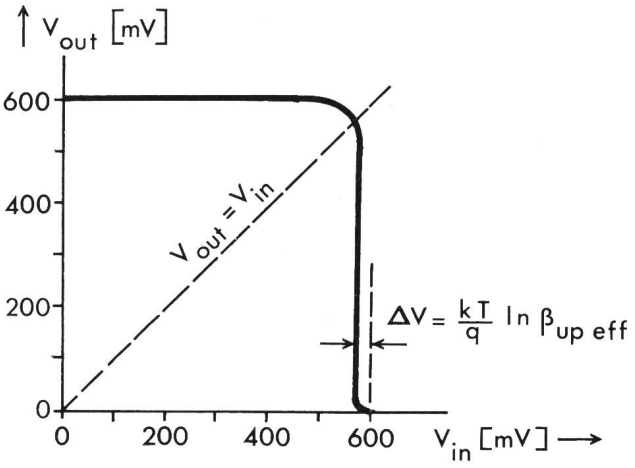

Fig. 6 Typical $V_{in} - V_{out}$ characteristic of an I²L inverter
It can be calculated that the voltage noise margin equals ΔV

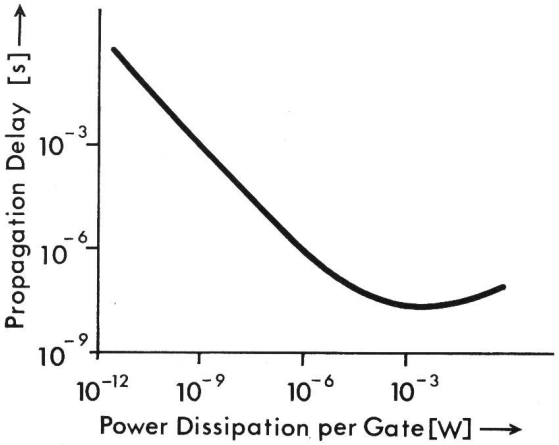

Fig. 7 Typical propagation delay of an I²L inverter versus power supplied to this inverter

the active charges in the transistors, of which the active charge in the common epiregion (hole storage) is by far the most important. These active charges are proportional to the current, and therefore the propagation delay is independent of the dissipation.

At high dissipation levels, above 1 mW, the series resistance of the base prevents fast charging and discharging of the active charges, and therefore the propagation delay time increases at increasing dissipation levels.

In multiple collector gates, the influence of the base series resistance increases for collectors which are further remote from injector and/or base contact than other collectors. Very often they don't reach the low horizontal part of the τD-curve and exhibit longer delay times. Fig. 8 shows the delay times versus power for the four collectors of a 4-collector-I²L-gate. For low power levels the delay-times are the same, for medium and high power levels a dispersion appears; the 4th collector which is the most remote collector from the injector becomes the slowest one. For worst case delay calculations in logic designs, the worst case delay time of the 4th collector must be taken.

At low dissipation levels, where the τD-product is proportional to CV^2, the speed and the τD-product can only be improved by decreasing the capacitance C. As C is proportional to the area of a gate, it is important to design the smallest gates possible. Power-delay products of 0.1 pJ have been demonstrated using 5 μm lay-out rules [4]; with still smaller lay-out rules even smaller τD-products can be reached.

The minimum delay time depends on $f_{T\,up\,npn}$, $\beta_{up\,eff}$, I_{p0}/I_{n0}, $f_{T\,pnp}$ and α_{pnp}. The ratio I_{p0}/I_{n0} not only determines $\beta_{up\,eff}$ but also indicates (as a back-injection factor) that for a part the low $f_{T\,pnp}$ must be taken into account in the switching speed calculations. This means that even in the case that $f_{T\,up\,npn}$ is extremely high, the switching speed is fully governed by $f_{T\,pnp}$ due to the back injection. The higher the I_{p0}/I_{n0} ratio, the more important the influence of the low $f_{T\,pnp}$ will be. Therefore, for a really high speed I²L technology, both the f_T's of the inverse operated npn *and* the lateral pnp must be increased.

The base series resistance can already influence the switching speed of the first collector. The switching speed of the 2nd, 3th and 4th collector is in any case affected by this series resistance at high power levels.

One remark must be made about the α of the pnp-transistor. At low power levels the α of the pnp transistor can be very near to 1 (which means that there is a good emitter efficiency and also a very low recombination in the pnp-base). At high

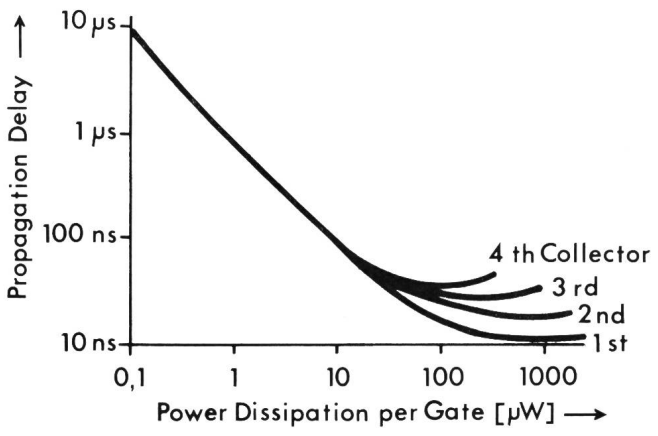

Fig. 8 Delay time versus power for a four-collector I²L gate

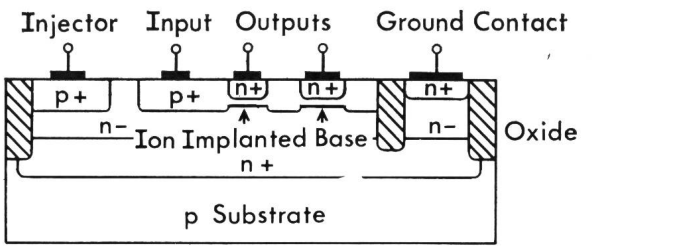

Fig. 9 Cross-section of a typical fast-I²L structure [8]
The epilayer is very thin (< 2 μm) and the isolation is a passive one (oxide)

power levels the α of the pnp decreases where the high injection effect is one of the occurring effects. This means that a reasonable part of the power supply current goes via the base of the pnp-transistor directly as a loss current to earth; sometimes this effect deviates the τD-curve earlier from the straight constant-τD-product-line than one should expect.

All the here described effects imply that the high power level behaviour of I²L is very complex and that very dedicated experiments must be done in order to discover all the different contributions of the various effects.

5. Fast I²L

As explained in the previous chapter, the minimum speed of I²L depends strongly on the cut-off frequencies of the inverse operated npn and pnp-transistors. In processes with a relatively thick epilayer (7...10 μm) the inverse operated npn-transistor is rather slow due to a considerable storage of holes which are injected from the base into the epilayer. This means that for these processes the maximum speed is in the range of 25...50 ns. In order to reach faster I²L, thinner epilayers have to be used; the thinner the epilayer, the faster the npn-transistor.

Together with a thin epilayer, oxide isolation can be used (Fig. 9) in order to eliminate side-wall capacitances. If at the same time, the lateral dimensions are decreased, a very dense I²L can be made with a low τD-product for the low power levels and with a short delay time at high power levels. Delay times of 3...5 ns have been reported [7...9], with τD-products in the range of 0.5 pJ. In one of the published high speed I²L processes, an extra loss diode is included [7], which fixes $\beta_{up\,eff}$ at a value of about 3 (too high a $\beta_{up\,eff}$ causes too much saturation and consequently a longer delay time). Preferably two base diffusions are made [7; 8]; a low doped diffusion (or ion implantation) for the intrinsic base and a high doped diffusion (or ion implantation) for the extrinsic base in order to keep the base series resistance as low as possible.

A switching speed of 3 ns seems to be the physical limit of I²L which is made with lateral pnp-transistors. The low $f_{T\,pnp}$ and a α-decrease at high power levels cause this limit.

6. Other types and technologies of I²L

Another way to manufacture I²L is to use a p-epilayer on a n^+-substrate. The p-epi forms the base of the npn-transistor and the pnp-transistor is made by two diffusions through one hole (Fig. 10). Power-delay products between 0.06 and 0.1 pJ, and a minimum delay time of 10 ns have been reported [10]. The analog circuits and other types of logic can be made on the same chip in this technology using the Collector Diffused Isolation (CDI) concept [11].

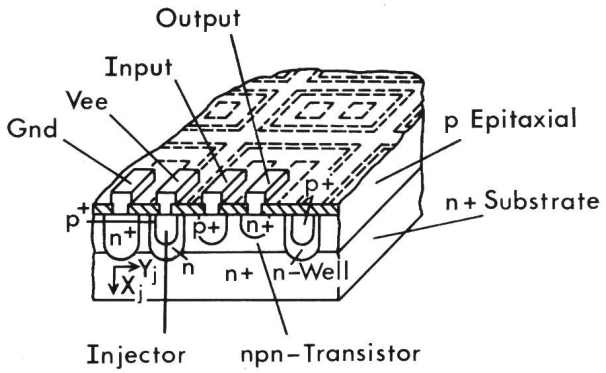

Fig. 10 Cross-section of an I²L technique by which the pnp-transistor is made with two diffusions through the same hole [10]
In this structure the pnp-base is made with the epilayer and is injected on four sides by the pnp-transistor

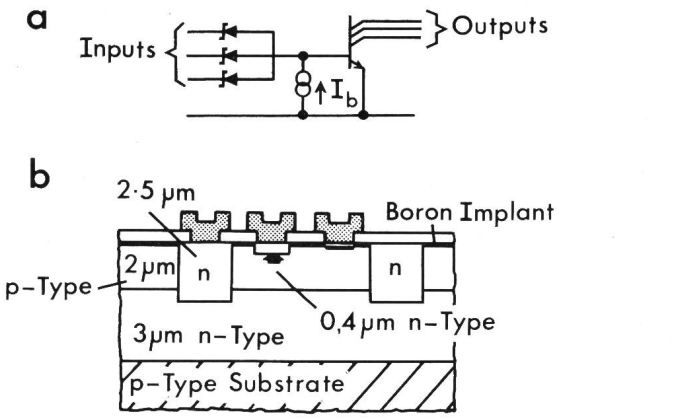

Fig. 11 Logic diagram (a) and Cross-section (b) of the SFL structure [12]

Quite different is the method of substrate fed I²L (SFL = Substrate Fed Logic) [12]. Here, two epitaxial layers are used on a heavily doped p-type substrate. The p-type epitaxial layer, which forms the base of the npn-transistor, is lightly doped, allowing the fabrication of Schottky contacts. This gives rise to an extremely powerful multi-input, multi-output logic element on a single base land. Fig. 11 shows the SFL scheme, and the SFL structure. The pnp transistor is a vertical one; the substrate is the emitter, the n-epilayer the base, and the p-epilayer the collector. Due to the compact structure and the low capacitances very low power delay products (0.05 pJ) have been measured [12]. However the low conductivity epilayers introduce large series resistances which implies that the minimum delay at high power levels is quite poor ($>$ 10 ns).

VIL (Vertical Injection Logic) [13] is a I²L type just between normal I²L and SFL. With an extra p-buried layer a vertical pnp is created which injects holes from this buried layer upwards to the base of the npn-transistor. A power delay product of 0.07 pJ and a minimum delay of about 9 ns have been reported.

Schottky I²L uses a Schottky diode in series with each collector in order to reduce the logic swing of the base of the I²L transistor [14...16]. As the τD-product is proportional to CV^2 a reduction of this product by a factor of 4 can be expected if the logic swing is reduced from about 700 mV to 300 mV. Improvements in this range have been measured. Fig. 12 gives the logical scheme of Schottky I²L. With a Schottky diode with a forward voltage of about 400 mV the reduced voltage swing is 300 mV indeed. The τD-product improvement exists in the low power range only. The minimum delay time is governed by active charge and series resistances; both will not be reduced by the Schottky diode in series with the collector.

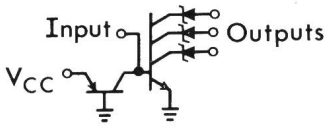

Fig. 12
Diagram of Schottky I²L

CHIL (Current Hogging Injection Logic) is a combination of I²L and Current Hogging Logic (CHL) [9; 17]. The addition of current hogging gates produces an I²L gate with more than one input gate, which makes the logic more powerful. Fig. 13 gives the cross-section. The higher τD-product ($>$ 1 pJ) and slower speed of CHL makes, that the combination of CHL and I²L does not lead to a fast logic with a very low power delay product. The manufacturing and the lay-out however are very simple, and in a thin epilayer process with oxide isolation, minimum delay times of 15 ns have been reached [9].

In Table I all power delay products (for the low power region) and all minimum delay times (for the high power region) of the described injection logic types are summarized.

Power delay product (τD) and minimum delay times (τ) of the described I²L types Table I

		τD-product low power region [p]	τ_{min} high power region [ns]
I²L; 10 µm clearances 7...10 µm epi	[1]	1...2	50
I²L; 5 µm clearances 5 µm epi	[1; 4]	0.1...0.4	25
I²L double diffused injector	[10]	0.06...0.1	10
SFL	[12]	0.05	10
VIL	[13]	0.07	9
Schottky I²L 10 µm epi	[16]	0.5...1	25...50
CHIL 1.5 µm epi	[9]	$>$ 1	15
Fast I²L 1...2 µm epi	[7...9]	$\approx$ 0.3	3...5

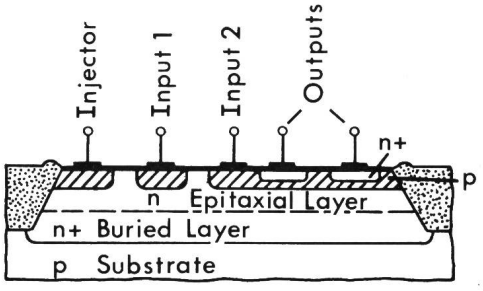

Fig. 13 Cross-section of a reported CHIL structure [9; 17]

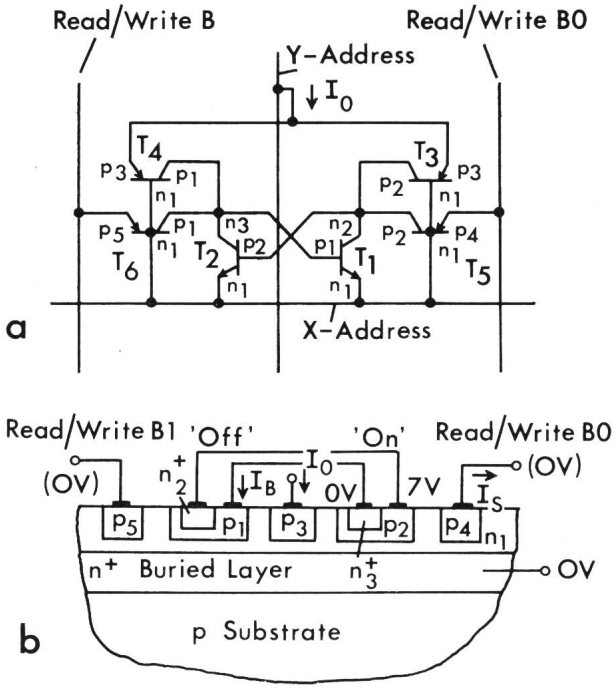

Fig. 14 Equivalent circuit diagram and cross-section of the structure of an injection-coupled RAM-cell [18]

7. Memories

I²L can be used successfully for both static and dynamic memories.

Fig. 14 shows the circuit diagram and a cross-section of a very small static memory cell [18]. This memory cell consists of two cross coupled I²L gates with a common injector for the power supply. Two extra pnp transistors form a connection to the read- and write-circuits. For reading, the outer pnp transistors are biased as collectors which partially collect the minority carriers that are injected by the ON-transistor into the adjacent n-region. Thus by sensing the differential currents in the bit lines it can be detected which of the npn transistors is ON. For writing, the cell power supply is momentarily turned off, and a current is supplied to the proper bit-line pnp. This causes a minority injection into the n-region which is partially collected by the p-base of the adjacent npn transistor, so that this transistor is turned on.

The cell is very small, viz. 2000 μm², which is equal to a packing density of 500 cells/mm². This cell size can be reduced to 700 μm² by applying passive (oxide) isolation. For a 4096-bit-chip an access time of about 50 ns has been predicted from measurements simulating a 64×64 array. The standby power is smaller than 0.1 μW/bit [18].

A similar static memory cell has been reported which requires no row-isolation diffusion, and for which the substrate is common for all the memory cells in the whole array [19]. In this design a double layer metallization is used. With a technology based on 7 μm line widths a packing density of 256 bit/mm² is achieved, and a standby current of 0.7 μW/bit has been measured. Complete selection, read- and write-circuitry are also given.

In contrast to the six-transistor static cell, a dynamic I²L can be made with only two transistors [20; 21]. The circuit diagram of the cell is shown in Fig. 15. A memory capacitance C_S is assumed to lie between the base and the collector of the npn-transistor (also between collector and base of the pnp-transistor, due to the merged structure). The capacitance C_S is charged during reading with a negative pulse at the W_n-line; a charge of β times the charge of the memory capacitance can be measured at the bit-line. Discharging C_S can be done selectively by applying the appropriate pulses on both the W_p-line and the bit-line in order to forward biase the merged pnp-transistor. The read-process is destructive; therefore, after reading, the right information has to be written back. In the standby state leakage currents affect the logic «1» state, which means that the cell must be refreshed (every 2 ms). Typically, the storage capacitance is about 0.1 pF, and the β of the npn-transistor is about 70, making the effective coupling capacitance about 7 pF, which is enough to assure an easily detectible logic swing of about 200 mV. The area of one cell can be very small (< 700 μm²).

Fully functional parts have been manufactured with 140 ns access time, 200 ns cycle time, 400 mW active power dissipation and 80 mW standby power. How this memory will compete with MOS dynamic memories is still an open question.

8. Interface circuits, TTL compatibility

The noise immunity of I²L is in general too low to interconnect I²L chips without noise-buffering interface circuits. As TTL circuits can be made on the same chip, it is advantageous to do so. This means that the I²L logic also can be combined with any other TTL circuit.

Generally a TTL load current is 1.9 mA per fan out for a low logic state and 20 μA or less for its high condition. Since an I²L gate operates at a current level between 1 and 20 μA per gate (in the low power range), two types of interface circuits are necessary: one at the gate inputs as an interface from TTL to I²L, and one at the gate output as an interface from I²L to TTL. The circuit diagram of the TTL/I²L interface is shown in Fig. 16. For the situation where the TTL gate is at its low logic level, the realization of the proper interface condition follows automatically, because a normal TTL input current will flow if appropriate resistor values are chosen. For the high logic TTL condition, however, care must be taken that the inverse current gain of I²L transistor T_1 does not affect the input current of the TTL transistor. Normally this inverse current gain has to be reasonably high for proper gate operation. The way around this dilemma is to short-circuit the collector-base junction of transistor T_1 in the interface circuit and add an extra diode T_2 to make the input threshold voltage again equal to the required TTL threshold voltage [5].

The interface from I²L to TTL can be made with current amplification stages. The lay-out of the current amplifier depends on the current level of I²L and on the number of TTL fan-outs required [5].

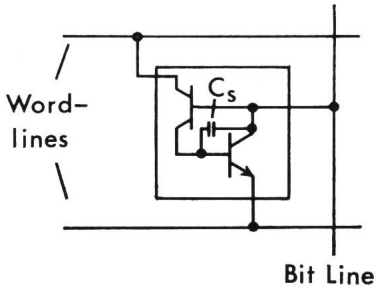

Fig. 15 Equivalent circuit diagram of a static I²L RAM-cell [20; 21]

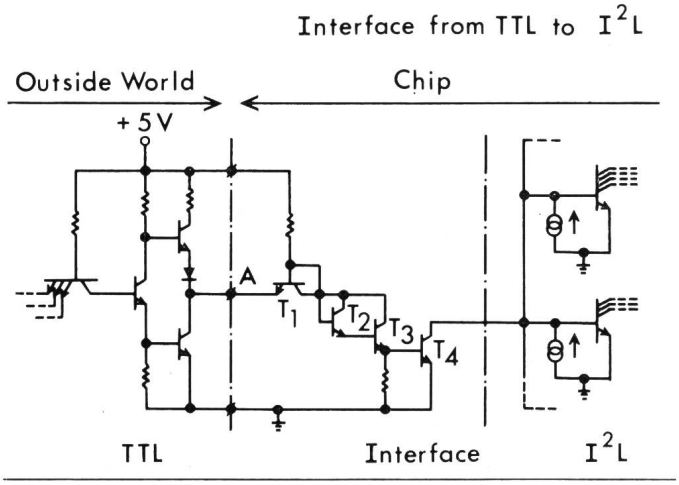

Fig. 16 Example of an I²L to TTL interface circuit
The current level of I²L is amplified to switch the high current level TTL circuitry. Transistors T_1 and T_2 serve as current amplifiers

9. Applications and conclusion

Applications for I²L are numerous. Watches, shutter circuits for camera's, digital-to-analog converters, digital voltmeter circuits, high frequency counters, digital tuners, read-only memories, shift registers, converters of all kinds, control logic for complex calculators, frequency deviders for electronic organs, remote control for TV-sets, microprocessors, telephone tone-dialing systems, alpha-numeric display circuits, motor-drive control, random access memories, timing controls, citizens' band radio circuits, phase-locked-loop circuits, automotive electronics, are only a small number of random choosen examples of I²L applications. Especially the combination with linear circuits makes I²L very suitable for small low cost systems.

I²L reduces a logic gate to a single complementary transistor pair. A vertical npn-transistor with multiple collectors as inverters and a lateral pnp-transistor serve both as current source and load, and no ohmic resistors are required for either source or load function. Packing densities up to 250 gates/mm² have been demonstrated. For speeds up to 50 ns existing bipolar technologies can be used; for higher speeds up to 3...5 ns new generation technologies have to be introduced.

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