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A 4.2-MHz Quartz Oscillator for Watch Applications

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Dans les montres-bracelets électroniques on utilise presque exclusivement des quartz 32 kHz. Les propriétés chronométriques peuvent encore être améliorées en recourant à des quartz de plusieurs MHz. Un circuit oscillateur est présenté qui permet la réalisation d'un ensemble oscillateur-diviseur NMOS, de fréquence élevée et de faible consommation.

In elektronischen Armbanduhren werden zurzeit überwiegend 32-kHz-Quarze verwendet. Die chronometrischen Eigenschaften können durch Einsatz hochfrequenter Quarze von einigen MHz weiter verbessert werden. Ein Oszillator wird beschrieben, der Teil eines NMOS-Oszillator-Frequenzteiler-Systems sein kann, das bei hohen Frequenzen einen niedrigen Stromverbrauch aufweist.

At the present time in nearly all electronic wrist watches 32-kHz-quartz crystals are used. The chronometric performance can be further improved by employing crystals of several MHz. An oscillator circuit is presented which can be used in a combined NMOS oscillator-frequency divider system in order to achieve low power consumption.

1. Introduction

At the present time in nearly all electronic wrist watches 32-kHz-quartz crystals are used. The chronometric performance can be further improved using a quartz of higher frequency, for example, an AT-cut crystal which has a particularly favorable frequency-temperature behavior. However, the problem of the increased current consumption which would occur, primarly in the frequency divider at the higher frequencies, must then be confronted.

2. The proposed approach

A solution can be found by resorting to an advanced technology which permits the use of components of very small dimensions. This paper presents another approach whereby consumption is kept low by use of a combined oscillator-divider system. In this circuitry approach

- all active elements are n-channel MOS transistors (carrier mobility in NMOS is higher than in PMOS devices), the passive elements being capacitors,
- the frequency divider is partially included in the resonant circuit of the oscillator.

If a divider concept is used [1] in which the stages are driven by two alternating voltages in phase opposition and whose amplitudes are relatively high (typically 1 V), the DC-current consumption due to the sequential charge of the node capacitances can be held low (about 1.5 µA to divide from 4.2 MHz). The alternating voltages are produced by the oscillator. In order to avoid too much current consumption in the latter its efficiency must be high.

A further reduction in current consumption can be achieved by connecting the oscillator and the divider in series, an arrangement facilitated by use of 3-V lithium cells (fig. 1).

Another technique used in the design is the polarization of the substrate relative to the circuit elements whereby the oscillator itself accomplishes this polarization [2]. As a result junction capacitances are reduced and positive and negative voltages can be used to control the transistors. In this way also a variation of the threshold voltage with temperature and threshold voltage differences between lots can be compensated.

After some considerations of certain basic oscillator circuits, details and results of an oscillator satisfying the requirements outlined will be presented.

This paper is an extended abstract of the lecture given at the Fall 1981 Meeting of the IEEE Swiss Section (Chapter on Solid State Devices and Circuits) on MOS Analog Circuits.

3. Considerations of some basic oscillator circuits

In order to obtain high voltages in an integrated oscillator with low power consumption the parallel resonance of the quartz should be used. In this case the power losses can be calculated by using the equivalent resistance of the quartz:

$$R_{pQ} = \frac{1}{\omega^2 (C_o + C_L)^2 R_s}$$

where C_o static capacitance of the quartz and the holder,
C_L capacitance of the circuitry parallel to the quartz,
R_s motional resistance of the quartz.

It should be mentioned that the motional resistance is related to the quality factor by

$$Q = 1/\omega C_s R_s$$

where C_s is the motional capacitance of the quartz.

The power dissipation in the quartz can be expressed by

$$P_Q = \frac{V_Q^2}{2 R_{pQ}} = \frac{1}{2} V_Q^2 \omega^2 (C_o + C_L)^2 R_s$$

where V_Q is the amplitude across the quartz. The motional resistance, the voltage and the sum of the parallel capacitances determine P_Q.

The power losses in the entire oscillator are composed of the one in the quartz (P_Q) and that in the driver circuit. It is also important to keep the latter low, which means that the driver circuit of the oscillator should have a high efficiency, this efficiency being defined by

$$\eta = P_Q/P_e$$

with $P_e = I_p V_p$

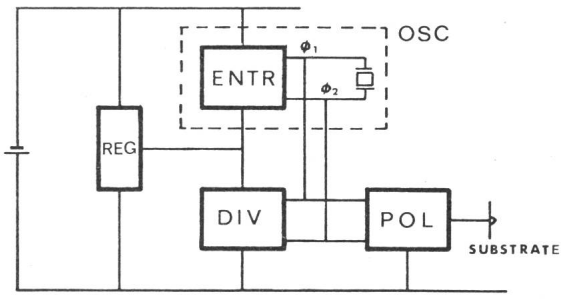

Fig. 1 Block diagram of a combined low power high-frequency oscillator-divider system

ENTR Driver circuit of the oscillator
DIV Frequency divider
POL Substrate polarization circuit
REG Supply voltage regulation circuit for the oscillator and divider connected in series

P_e being the power consumption, V_p the supply voltage and I_p the supply current of the oscillator.

Some basic oscillator circuits are presented in the figures 2a to 2d.

The classical three-point circuit (fig. 2a) contains only one active element. In any case, the efficiency is lower than 0.5. The circuit 2b employs the well known CMOS inverter [3; 4]. The amplitude of the fundamental component of the current is doubled in respect to the circuit 2a. Consequently, the efficiency can reach almost 1. The peak to peak value of the output voltage is limited by the supply voltage.

In the circuit 2c both transistors are of the same type of conductivity. The opposition of phase of the currents is obtained by the phase opposition of the gate voltages. If this circuit is polarized with respect to the substrate, two voltages in phase opposition can be produced whose peak to peak value can be higher than the supply voltage.

4. The symmetrical NMOS oscillator

The symmetrical version of this circuit (fig. 2d) has the advantage of being less sensitive to asymmetrical loading [5]. In integrated form it occupies about the same area as circuit 2c due to the reduction by one half of the transconductance of the transistors and the size of the capacitors. In circuit 2d, the amplitude of both voltages in phase opposition, appearing on the points a and a′, is given by

$$V_a = V_Q/2 = V_b\,(1 + C_2/C_1)$$

where the amplitude V_b (on b and b′) may nearly become $V_p/2$. By selecting capacitances such that $C_1/C_2 = C_4/C_3$ all four transistors have the same gate voltage. In this case, each transistor supplies the same energy P_T for maintaining the oscillation:

$$P_T = \frac{1}{2}\, i_f\, V_b$$

where i_f is the amplitude of the fundamental component of the current pulses delivered by each transistor.

In each pair of transistors (1, 2 and 1′, 2′) flows a current with a DC component I_b. The power consumption of the oscillator becomes

$$P_e = 2\, I_b\, V_p$$

and the efficiency can be expressed by

$$\eta = \frac{P_Q}{P_e} = \frac{4\, P_T}{P_e} = \frac{i_f\, V_b}{I_b\, V_p}$$

The ratio i_f/I_b can be calculated by Fourier analysis. For small conduction angles of current, and considering the quadratic caracteristic of transistors or their exponential behavior in the weak inversion region with gate voltage greater than 0.2 V, the value of i_f/I_b is nearly 2. Under these conditions the efficiency becomes

$$\eta \approx 2\, V_b/V_p$$

These latter considerations are valid only if the transistors are not overdriven, i.e. if they are held in the current saturation region. This condition can always be satisfied using the circuit of figure 3 which determines the operating point of the driver transistors.

4.1 Operating point determination of the driver transistors and amplitude regulation

The gate voltage of the driver transistors is limited with respect to V_p (transistor 1) and $V_{b\,min}$ (transistor 2) due to the transistors D. The dimensions of the latter and the current delivered by the generators G_1 and G_2 can be arranged in order to limit the gate voltages exceeding the extrapolated threshold voltage V_T to the minimum value $V_{DS\,min}$ of the respective drain-source voltages. In this way, the driver transistors always remain in saturation.

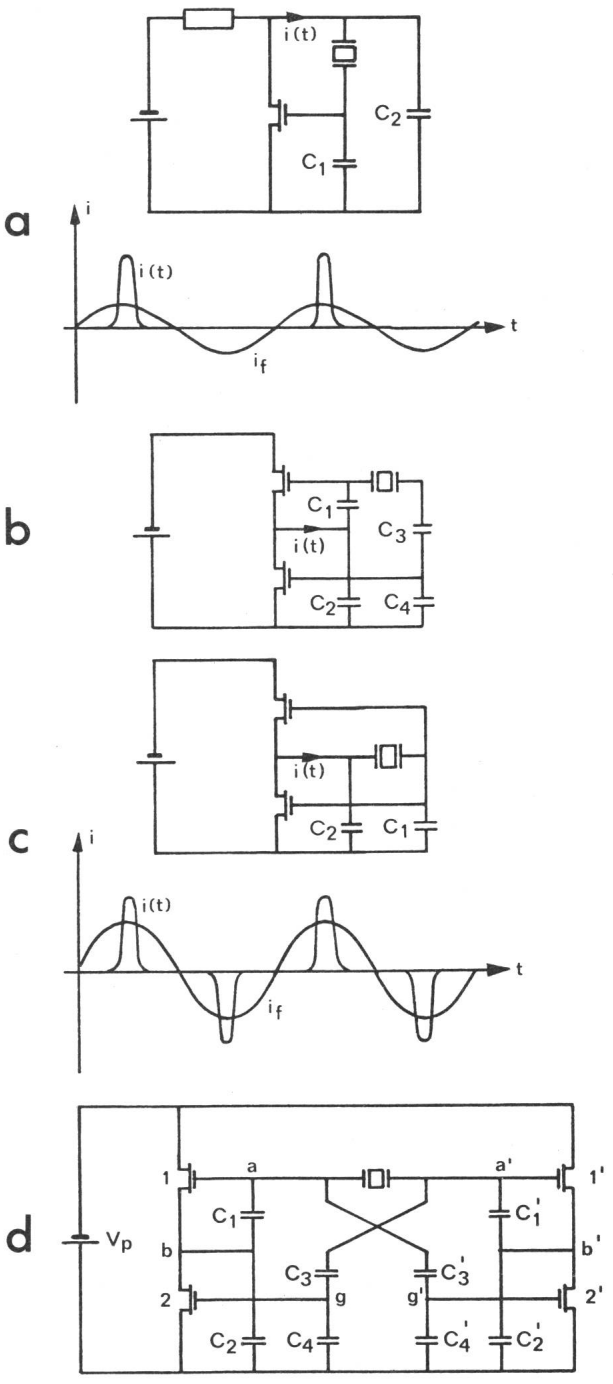

Fig. 2 Basic oscillator circuits

$i(t)$ driving current for the resonant circuit
i_f fundamental component of $i(t)$

a Circuit with one active element
b Circuit with CMOS inverter
c Circuit with two MOS transistors of the same conductivity type
d Symmetrical version of circuit c

Because of this limitation by the transistors D the angle of current conduction of the driver transistors decreases with increasing amplitude. Therefore the mean transconductance S_m decreases, transconductance defined by

$$S_m = i_f / V_g$$

where V_g is the amplitude of the gate voltage. With this arrangement a highly efficient amplitude stabilization is achieved without overdriving the transistors.

In the equilibrium oscillation state the condition

$$S_m r_b = \frac{V_b}{V_g} = \frac{C_1}{C_2}$$

is satisfield, whereby r_b is the equivalent resistance of the quartz loading each of the driver transistors.

This equivalent resistance transformed to points b an b′ can be expressed by

$$r_{bQ} \approx \frac{1}{2} R_{pQ} \left(\frac{C_1}{C_1 + C_2} \right)^2$$

and the resistance loading each transistor is then

$$r_b = 2\, r_{bQ}.$$

In the equilibrium state the voltage V_b depends primarly on the supply voltage and its amplitude is nearly $V_p/2$. This amplitude varies only slightly with changes of loss in the resonance circuit. In fact, for a supply voltage of 1.5 V, an equivalent resistance of the resonant circuit of 2.3 MΩ and with driver transistor transconductance of 200 μA/V² the peak to peak value of V_b is about 1.25 V ($\eta = 0.83$). Doubling the load (1.15 MΩ) reduces V_b by only 5 %. The same value results if the transconductance of the driver transistors is halved.

It should be emphasized that in this oscillator circuit the transistors operate under optimum biasing conditions, regardless of the load, transconductances or threshold voltages. In any case the oscillator then furnishes the maximum possible output voltage without overdriving the transistors.

4.2 Substrate polarization circuit

It has been mentioned that substrate is polarized with respect to the circuit. For the oscillator this is a necessity since the gate voltage swing of the driver transistors can become negative with respect to the minus pole of the supply cell. As explained, the threshold voltage can then be regulated to a fixed low value by means of this polarization. This is important for the frequency divider and also for the current generators in the oscillator.

The function of the polarization circuit is as follows (fig. 4). A voltage generator M (Schenkel-type voltage multiplier [6]) supplies the reference transistor R (gate connected to source) and a current generator G, which are connected in series [7; 8]. Without polarization the threshold voltage is negative; in this case the current of the transistor R is greater than that delivered by generator G. The excess current charges the capacitor C via both voltage generators M. The voltage generated in this way between the common point 0 and the substrate influences the caracteristics of the transistor R, its threshold voltage becomes more positive and the current flowing across it diminishes finally to that of the current generator. As a result all circuit elements connected to the common point 0 are polarized with respect to the substrate.

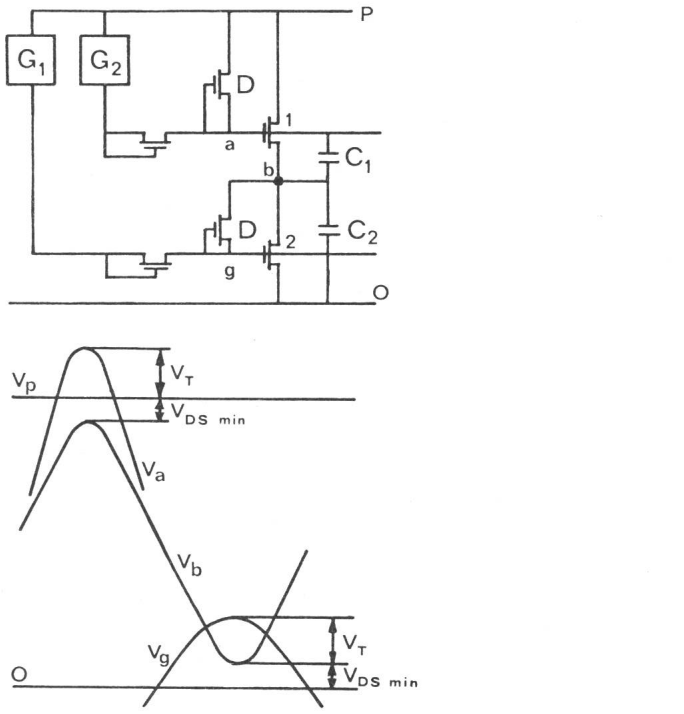

Fig. 3 Circuit determining the operating point of the driver transistors

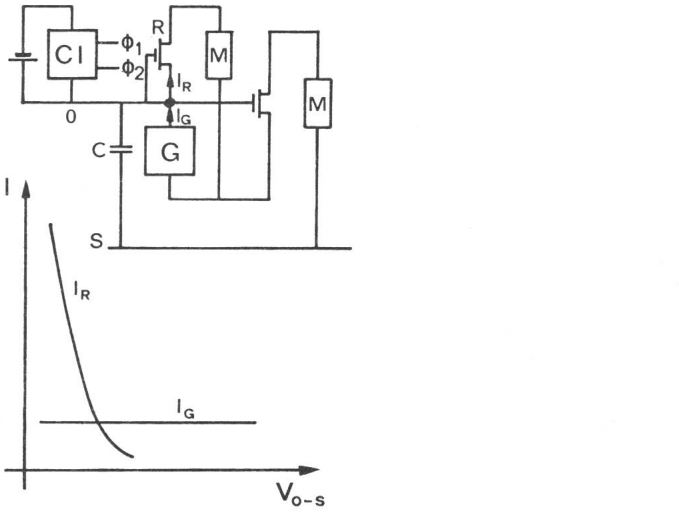

Fig. 4 Substrate polarization circuit

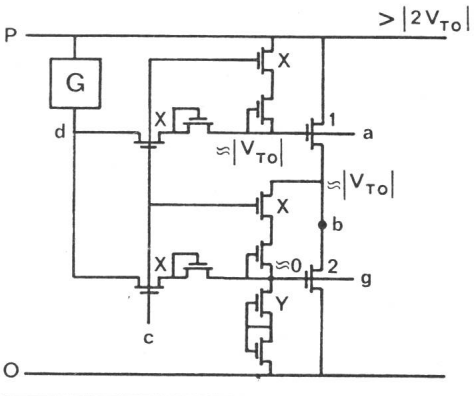

Fig. 5 Circuit assuring the starting of the oscillator

The current of generator G can be some tens of nA. The current of the transistors in the IC whose source is connected to the common point 0 will be that of the transistor R, multiplied by the respective length/width ratios, if their gate voltage is zero. For example, with $I_G = 20$ nA, W_R (channel width of transistor R) = 200 µm the current across 10 µm wide transistors in the IC will be 1 nA if the channel lengths are the same.

4.3 Starting conditions

When using such a polarizing circuit it must be remembered that the substrate is not polarized when the system is first switched on. Consequently, the oscillator must begin to function with a non-polarized substrate and must be able to deliver the two alternating voltages in phase opposition to polarize the circuit.

When initially energized, the threshold voltage of the transistors is negative, i.e. they are conducting with zero gate voltage. In order to ensure an oscillator starting under conditions of relatively heavy loads, the driver transistors must initially be in saturation. Also the components connected to the gate of these transistors must have high impedance.

Many arrangements can be found to assume these conditions, one of which is shown in figure 5.

The gates of the transistors X are connected to the output of a Schenkel-type voltage multiplier, supplied by V_b an V_b'. Without oscillation, no output voltage appears on point c. The current generator G presents a relatively low resistive path between the points d and P, the potential on d is about the same as on P. Point d constitutes the drain of the transistors relying this point to the gates of the driver transistors 1 and 2 via other transistors connected in a diode configuration and which are strongly conducting.

The potential on the gate of driver transistor 1 will be charged to $|V_{TO}|$, which is the absolute value of the (negative) threshold voltage. The ratio of the transconductances of transistors X and Y can be chosen such as to fix the gate potential of transistor 2 near to zero. Because of the negative threshold voltage a starting current flows across transistor 2. The same current must flow across transistor 1, therefore, the potential on point b approaches $|V_{TO}|$. Under these conditions both driver transistors are in the desired saturation region.

The same arrangement as shown can be used to bias transistors 1′ and 2′, the generator G being common.

5. Experimental results

The NMOS oscillator described was realized in a metal-gate technology with transistors having a minimum channel length of about 10 µm. It occupies ≈ 0.4 mm², including the polarization circuit.

For evaluation two kinds of circuits were integrated: the oscillator alone where the polarization is done by external biasing and the complete oscillator-polarization circuitry. They were both laid out for a supply voltage of 1.5 V. Measurements were carried out using 4.2 MHz crystals with a motional capacitance of about 6 fF.

The first diagram (fig. 6a) shows the current consumption of an oscillator as a function of the substrate polarization voltage. In the same diagram is shown the extrapolated thresholdvoltage as function of the polarization. It appears that the oscillator works with a current less than 1 µA in the threshold region from 0.2 to higher than 0.5 V. This voltage range is more than sufficient since threshold voltage will be regulated to about 0.25 V.

The dependence of the current consumption on the supply voltage appears in diagram 6b. As reported, the system works down to 1 V. Above this value the substrate is polarized correctly. As it can be expected, the current consumption increases linearly with the supply voltage.

In accordance with the relations derived for the power losses in the quartz and for the efficiency, the current consumption can be expressed as

$$I_p = \frac{2\,V_a^2}{V_p}\,\frac{\omega^2\,(C_o + C_L)^2\,R_s}{\eta} = \frac{2\,V_a^2}{V_p}\,\frac{\omega\,(C_o + C_L)^2}{C_s\,Q\,\eta}$$

This relation was verified by measuring an oscillator and an oscillator-polarization assembly with two different quartz crystals. By varying $C_o + C_L$ (diagram 6c) the efficiency can be deduced:

$$\eta \approx \frac{2\,V_a^2}{V_p}\,\frac{\omega}{C_s\,Q}\,\frac{\Delta\,(C_o + C_L)^2}{\Delta\,I_p}$$

The experimental value determined was 0.71, which corresponds well to the calculed value.

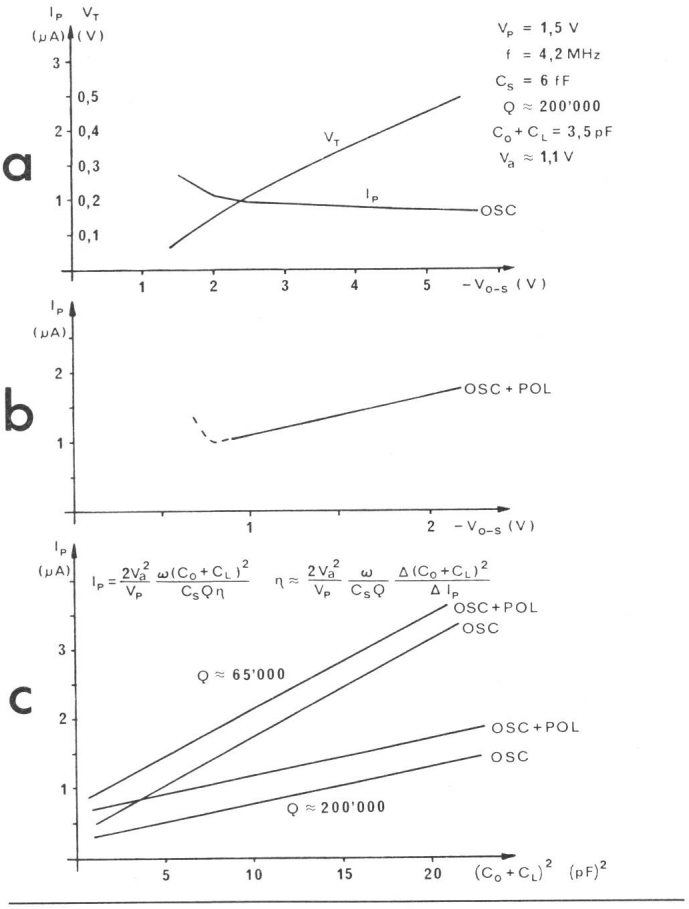

Fig. 6 Experimental results of integrated oscillators

a Current consumption I_p of an oscillator and threshold voltage V_T vs. substrate polarization voltage

b Current consumption I_p of a complete oscillator-polarization circuitry vs. supply voltage V_p

c Current consumption I_p vs. $(C_o + C_L)^2$
C_o Static capacitance of the quartz and the holder
C_L Capacitance of the circuitry parallel to the quartz

It can be seen in diagram 6c that the polarization circuit is responsible for an additional current consumption of about 0.4 μA and that a consumption of about 0.3 μA also exists which is probably caused by losses in the substrate.

The concept presented here leads to an efficient system for dividing the frequency down to 32 kHz – a widely used operating frequency. The lower frequencies can be divided by conventional CMOS stages. In such an assembly the high frequency NMOS part could be integrated in a p-well which would be polarized.

The use of more complex technologies (silicon-gate with two poly layers, for example) would permit a further reduction in the current consumption.

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