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A 1.5 V Only CMOS EEPROM based on Fowler-Nordheim Emission — Design, Technology and Applications

J. C. Martin and B. Gerber

The paper describes the CMOS process by which digital and analog custom circuits are produced, including non-volatile memories. Two types of memory cells are presented. The test circuits and the applications shown include 10 to 50 bits and have a very low current consumption (some μA at 1.5 V).

Description du procédé CMOS permettant la réalisation de circuits digitaux et analogiques à la demande, y compris des mémoires non volatiles. Deux cellules de mémoires sont proposées. Les circuits tests et applications présentés comprennent de 10 à 50 bits et sont à très faible consommation (quelques μA à 1,5 V).

Ein CMOS-Prozess wird beschrieben, mit dem digitale und analoge Schaltungen nach Kundenspezifikation, auch nicht-flüchtige Speicher, hergestellt werden. Es werden zwei Speicherzellen erläutert. Die vorgestellten Prüfschaltungen und Anwendungen umfassen 10 bis 50 Bit und haben einen sehr geringen Stromverbrauch (einige μA bei 1,5 V).

This paper has been presented at the 6th IEEE Non-Volatile Semiconductor Memory Workshop, August 1983, Vail, Colorado, and at the Fall 1983 Meeting, of the IEEE Chapter on Solid-State Devices and Circuits October 1983, Bern.

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1. Introduction

Since 1976, the CEH[1]) has devoted 7 man-years to R & D on non-volatile semiconductor memories. Our interest was not to design or to produce a 64 kbit EEPROM (Electrically Erasable and Programmable Read-Only-Memory) as has been done by several other semiconductor Companies, but to demonstrate the feasibility of a low power and low voltage EEPROM. We will describe the low voltage CMOS process, compatible with the one used for digital and analog circuits, two types of memory cells and several other circuits. The applications shown in this paper do not need more than 10 to 50 bits and are part of full custom circuits.

Note that we use a p-ch EEPROM because our CMOS technology is a p-well process which enables operation at high negative voltage. Further, we have replaced the p^+-n avalanche injection for writing the FAMOS cell [1; 2; 3] by Fowler-Nordheim emission which consumes less power and is better adapted to on-chip voltage multipliers.

2. Process description

The 1.5 V double polysilicon, 10 mask CMOS process, is a fully implanted p-well process. Figure 1 shows the main steps of the fabrication. It starts with a 15...35 Ωcm n-type ‹100› wafer which is phosphorus implanted. The first mask defines the p-well region which is boron implanted. The second mask is an extra step for the EEPROM and allows Fowler-Nordheim emission as write mechanism. It consists of implanting a p^+region in the substrate. Then, complete oxide removal is followed by the field oxide growth. The third mask defines the source-drain-gate regions of all transistors. An injection oxide of 28 nm is grown. This is followed by the first polysilicon layer deposition which is n^+ doped. The fourth mask defines the geometry of the first polysilicon layer. This layer is used as floating gate of EEPROM cells and as bottom plate of poly-poly high value capacitors. Then, a 100 nm thick gate oxide is grown, followed by the deposition of the second polysilicon layer. The fifth mask defines geometries of the second polysilicon layer which is used for p and n-channel transistor gates, interconnections, control electrodes of EEPROM cells, top plates of poly-poly capacitors and polysilicon lateral diodes created by the sixth and seventh mask. These masks define p^+ and n^+ regions in the poly-Si layers and in the mono-Si, mainly the sources and drains of MOS transistors. Mask 8 opens contact windows through the oxide (contact to the p^+ diffusion, as well as to the first or second poly-Si layer). Mask 9 defines the aluminum geometries (connections and bonding pads). The tenth mask opens contact windows to the bonding pads through the silicon nitride scratch protection layer.

Several remarks should be made: the injection oxide is the key of the EEPROM cell; it is the oxide through which the electrons can "travel" for writing and erasing, forming at the same time the barrier, essential to the retention of information. This oxide is not chemically attacked prior to the first polysilicon deposition.

Furthermore, the process is a bi-doped one. The second poly-Si layer is doped p^+ for the p-channel transistors and n^+ for the n-channel transistors. Therefore, no channel implant is necessary to achieve threshold voltages of approximately 0.5 V.

The bi-doped approach yields an interesting circuit element as shown in

[1]) Centre Electronique Horloger S.A., Neuchâtel

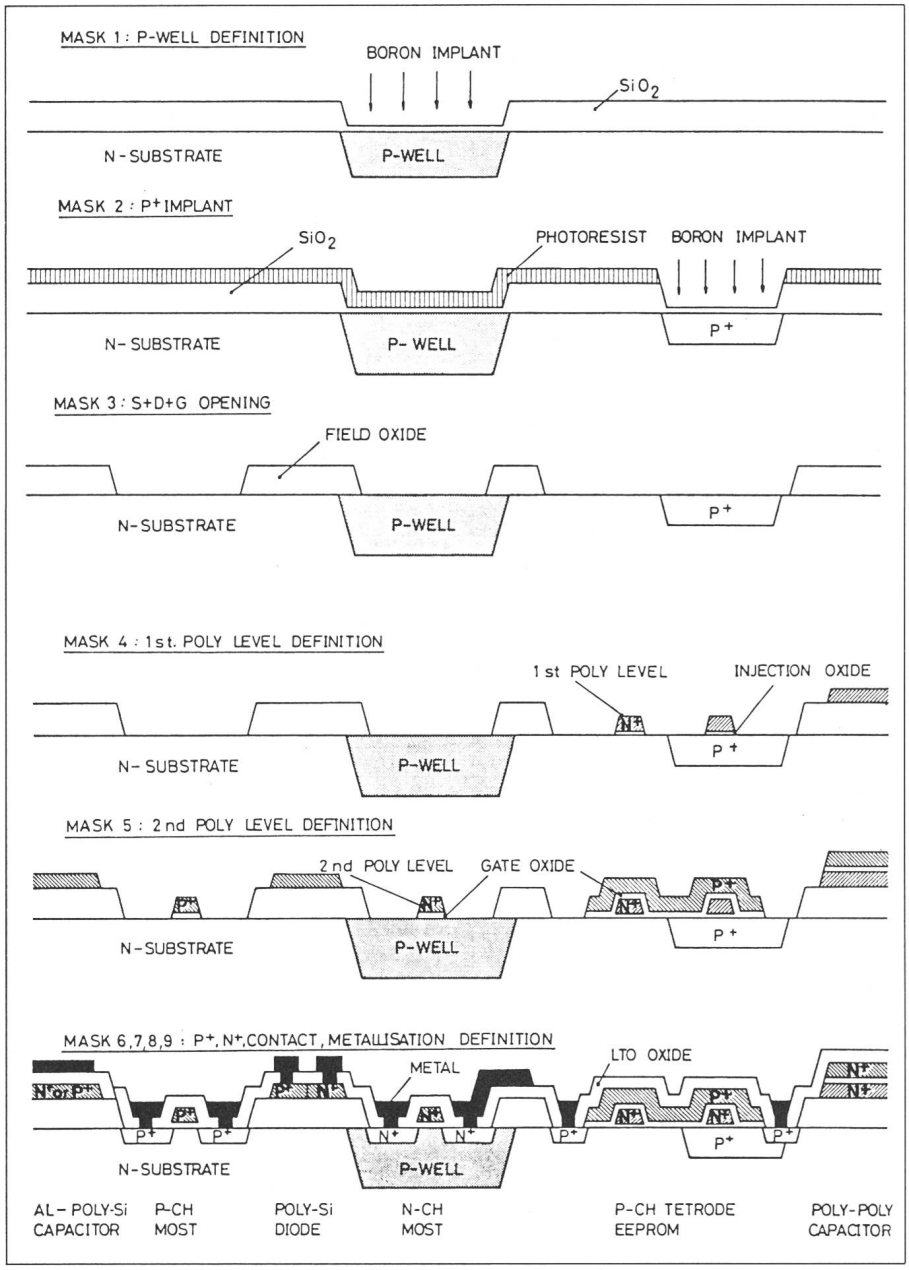


Fig. 1 1.5 V 10 mask CMOS process

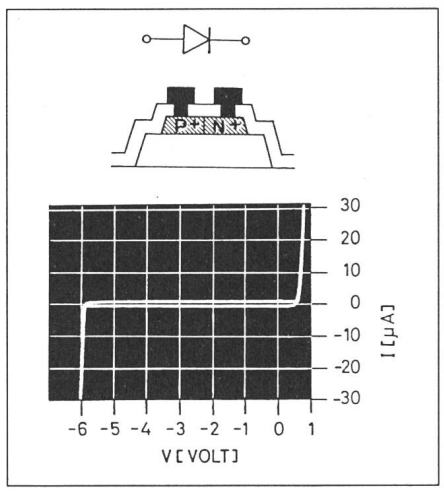


Fig. 2 I-V Characteristic of a Poly-Si Diode

figure 2, the floating polysilicon diodes, which are automatically formed at the interface between p^+ and n^+ doped polysilicon. The *I-V* curve shows a breakdown voltage at about 6 V; the reverse current is typically of 0.1...1 nA at 1.5 V for a 6 µm wide diode. These diodes are used in the voltage multiplier [2; 3] and also as a high value resistive bias element in the design of analog circuits.

Finally, parasitic transistors appear at voltages as low as 5 V. Channel stoppers are therefore needed for the interconnections operating at high voltages, e.g. in the voltage multiplier, in the interfaces and in the memory cells. The drain avalanche breakdown

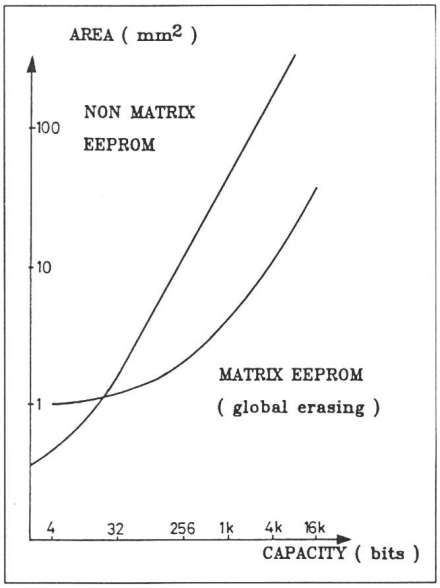


Fig. 3 Non-matrix and matrix EEPROM, comparison of area

of n-channel transistors is used to limit this high voltage to about 28 V.

3. Memory cells

The usual organization of memories like ROM's an RAM's is an array of cells with a decoder and a multiplexer. The random access allows the minimization of peripheral circuits [4]. Furthermore we economize circuits like read amplifiers thanks to the fact that we only need one for each bit of a word.

For our small capacity memory, we propose two kinds of cells, the non-matrix one and the matrix one. For a small number of bits, or when we need access simultaneously to all bits (one word memory) the non-matrix organization has been chosen. Figure 3 compares the memory area as a function of the number of bits. The non-matrix EEPROM has direct access to all bits, the matrix one is evaluated for a 4 bit word. The crossover lies at about 20 bits. Figure 4 shows that a non-matrix

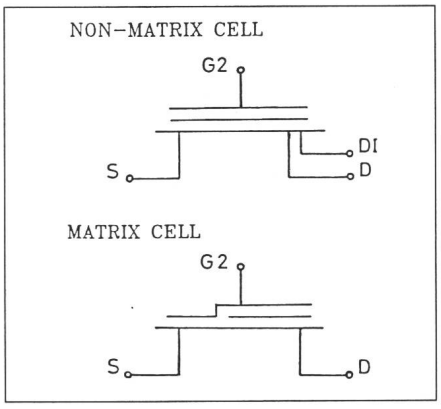


Fig. 4 EEPROM cells

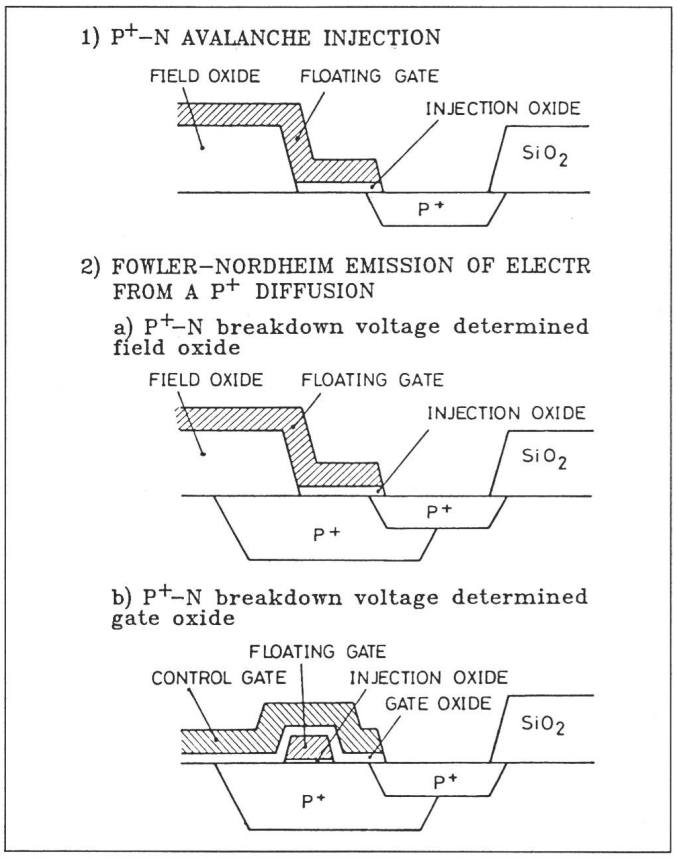


Fig. 5
Fowler-Nordheim emission of electrons from a p^+ diffusion

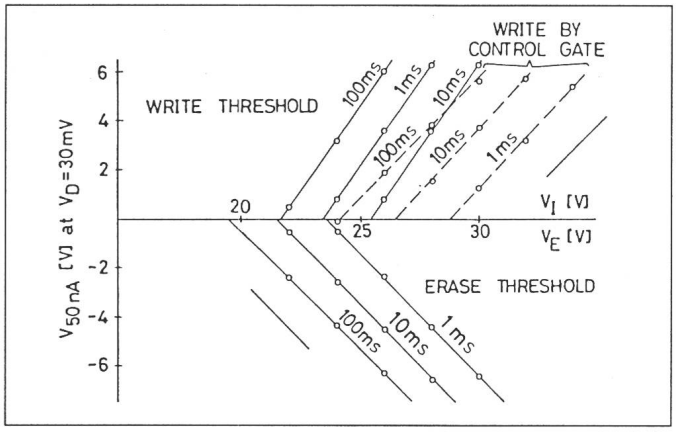


Fig. 7 EEPROM non-matrix cell: write and erase threshold voltages versus programming voltage

cell is a 4-terminal device with drain, source and control gate electrodes plus an injector drain, and that a matrix cell is a 3-terminal device realized in the form of a tetrode.

Figure 5 describes the physical mechanism used in these kinds of cells to write (or to charge) the floating gate with electrons. The p^+-n avalanche injection, previously used [2; 3], leads to a relatively poor endurance due to trapped charges in the injection oxide, and to a relatively high current during writing. The structure, allowing Fowler-Nordheim emission described in the second part of figure 5 is obtained by extending the p^+ region by an extra diffusion as far as the field oxide in non-matrix cells (a) and up to the 100 nm gate oxide in matrix cells (b). The injection of electrons occurs at a voltage below the avalanche breakdown of the p^+-n junction. The p^+ extension corresponds to the extra p^+ implant defined by mask 2 of the process description.

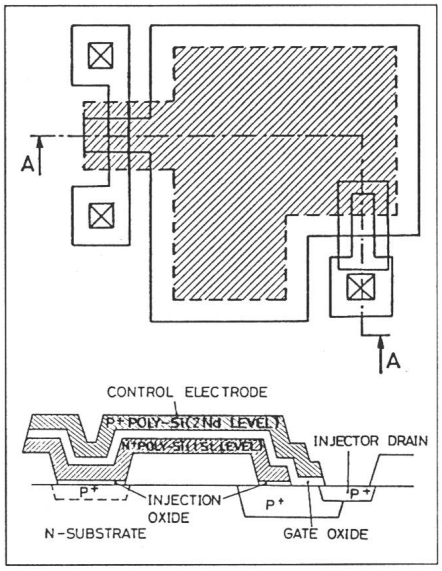


Fig. 6 EEPROM non-matrix cell

4. Non-matrix cell

Figure 6 shows a top view and a section of the non-matrix cell. It is a p-channel stacked gate structure with an n^+-doped floating polysilicon gate which is realized with the first polysilicon layer. The injection oxide thickness is 28 nm and the gate oxide also used between floating gate and control electrode is 100 nm. The capacitor coupling ratio between floating gate and control electrode is 0.8.

Writing the memory is performed by applying a −28 V voltage pulse to the injector drain and maintaining the control electrode at 0 V. Electrons are injected into the floating gate by Fowler-Nordheim emission. The floating gate is charged negatively and the transistor is conducting.

Erasing is obtained by applying the same voltage pulse to the control electrode. The injector drain is grounded or floating. Electrons of the floating gate are reinjected through the same oxide towards substrate and p^+ injector by Fowler-Nordheim emission.

Figure 7 shows the measured characteristics of a non-matrix cell: the threshold voltage is defined as being the control gate voltage necessary to produce a channel current of 50 nA with a drain to source polarization of −30 mV. The parameters are the programming and erasing voltages (V_I and V_E) and the programming time. The threshold voltage is proportional to the height of the voltage pulse. On the same figure the write threshold voltage obtained with a positive pulse on the control gate has been reported. The different slopes of the curves are probably due to voltage losses either in the polysilicon or in the bulk during writing.

Figure 8 shows the possibility of recording the channel current during

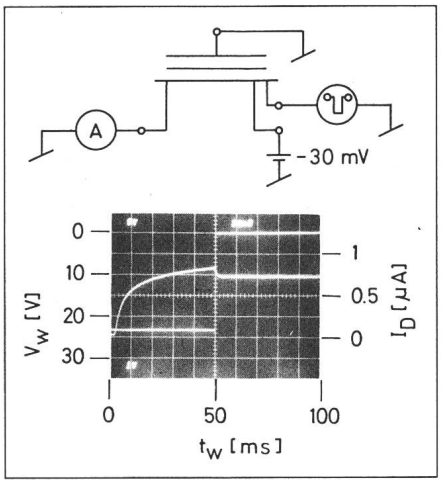


Fig. 8 EEPROM non-matrix cell: drain current evolution during writing

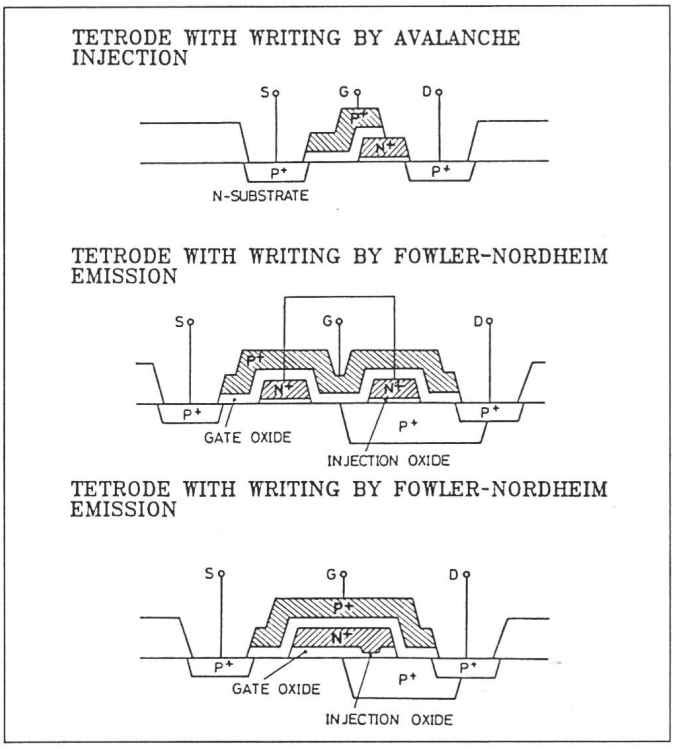


Fig. 9
EEPROM matrix cells

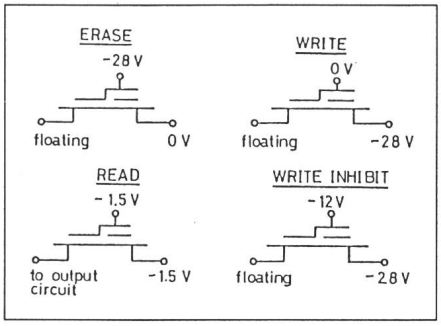


Fig. 10 Matrix cell
Erase, write, write inhibit and read configuration

writing. One can imagine the implementation of an adjustable resistor or an analog EEPROM, and this is one goal for further developments [5]. Note the 10% decrease of the drain current at the end of the pulse. It corresponds to a capacitive coupling between injector and floating gate.

5. Matrix cell

Figure 9 (middle part) shows the matrix cell, consisting of the following elements, from left to right: the source (S), the selection transistor (gate oxide) with the control electrode (G) as gate, the read transistor with the floating gate (electrically in series with the selection transistor), finally the writing part (injection oxide) comprizing the special p^+ region electrically connected to the drain (D). Figure 9 (upper part) depicts the cell in the avalanche writing version [2; 3]. Figure 9 (bottom part) shows another tetrode configuration requiring an additional masking step to define the injection area.

Compared to non-matrix cells, the principal differences are the merger of the drain and the injection drain, saving one line, and the additional transistor electrically in series with the read transistor for the cell selection in a matrix configuration.

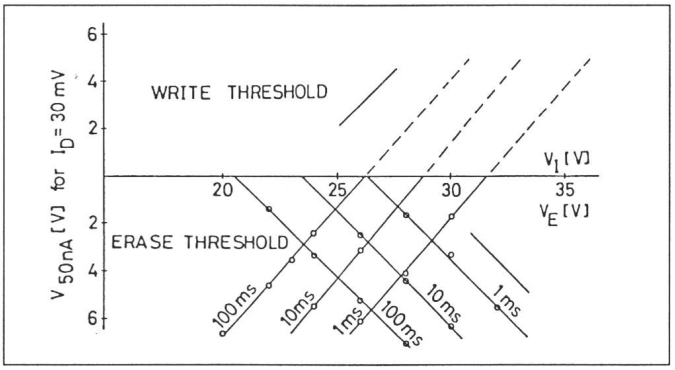
Figure 10 shows the row and line voltages needed to operate the memory cell. Note that the write inhibit condition is assured by an intermediate voltage level (−12 V) at the control electrode.

Figure 11 shows the measured characteristics corresponding to those of the non-matrix cell in figure 7. Note that, due to the selection transistor in series with the read transistor, the threshold voltage obtained after writing cannot be directly measured.

6. Test circuits

Figure 12 shows a 13 bit EEPROM non-matrix cell memory developed for digital tuning applications. The circuit diagram (fig. 12a) represents a voltage multiplier using the polysilicon diodes of figure 2, the EEPROM with its input and output circuits [3]. A 100 ms pulse can write or erase an arbitrary number of bits in this circuit with a 32 kHz clock frequency. The single power supply (V_{cc}) provides only 1.5 V and 3 µA. Figure 12b is the microphotograph of the circuit.

Fig. 11
EEPROM matrix cell: write and erase threshold voltages versus programming voltage



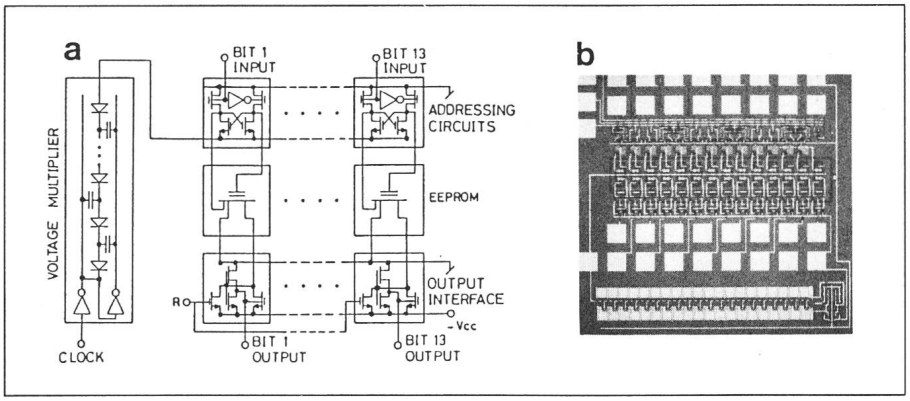


Fig. 12 13-bit EEPROM memory
On the microphotograph (b) the multiplier is to be seen at the bottom, the input and output circuits at the centre

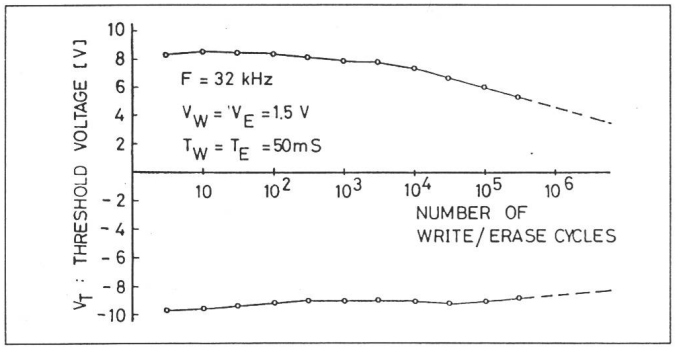


Fig. 13
Endurance of a non-matrix cell

Figure 13 shows the measured endurance of this test circuit: the write and erase threshold voltages are a function of the number of cycles. It can be extrapolated that, after 10^6 cycles, the write threshold voltage will drop to half of its initial value. Ten years of retention at 70 °C does not seem to be a problem.

Figure 14 shows a microphotograph of a 7×6 bit matrix cell EEPROM. It is integrated with a modified technology and 4 μm design rules. It is word erasable needing a single decoder (no multiplexer) and two voltage multipliers, one for the bit lines, and the other one for the word lines. Write, erase and read times are 100, 100 and 2 ms respectively. More than 1 million cycles have been reached with the first circuits.

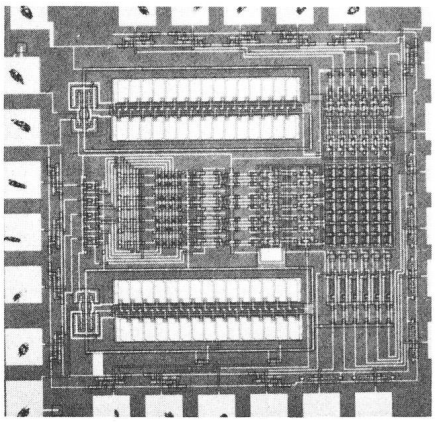


Fig. 14 Microphotograph of a 7×6 bit EEPROM

7. Applications

The non-matrix cells can be used for digital tuning of an electronic watch [6]: Taking a non-adjusted quartz crystal and adjusting the dividing ratio of a divider chain by pulse suppression allows to obtain the correct frequency at the output for driving the watch. The number of pulses to be suppressed is stored in a 13 bit/1.5 V non-volatile memory. Thus, this vital information will not be lost during battery replacement. Figure 15 is a microphotograph of such a watch circuit, chip area is 8 mm² and the memory block occupies about 1 mm². The quartz frequency is 0.5 MHz and the total power consumption is less than 2 μA.

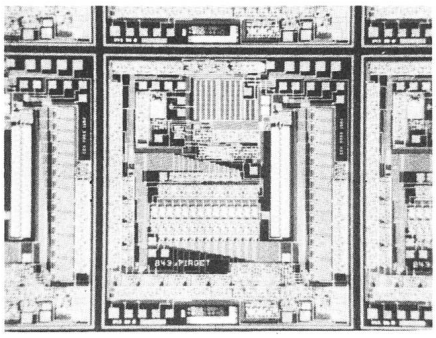


Fig. 15 Microphotograph of a watch circuit including the 13-bit EEPROM of figure 12

Another example of digital tuning concerns the thermally compensated watch. One can adjust this compensation in regard to the real frequency temperature characteristic of the quartz and store the result in a non-volatile memory.

A lot of other applications are open such as current or voltage reference adjustment, programming the gain of amplifiers and the bandwidth of filters, etc. In a microcomputer structure, with its application program stored in a ROM, one can use an EEPROM for part of data, thus conserving the most important information during power supply loss.

8. Conclusions

Non-matrix (1...20 bit) and matrix (20...50 bit) memory cells are available and compatible with our low voltage and low power technology. Fowler-Nordheim emission for both writing and erasing is used and very good endurance has been obtained.

The possibility of including EEPROM's without degrading other technological parameters opens new possibilities in the design and realization of analog and digital circuits.

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