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# A Single Chip Microcomputer with EEPROM

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*The architecture of a microcomputer with an on-chip EEPROM is presented. The EEPROM device performances and new applications for this type of circuit are described.*

*L'auteur présente l'architecture d'un microprocesseur avec une EEPROM sur une seule puce. Les performances de l'EEPROM sont décrites ainsi que de nouvelles applications de ce type de circuit.*

*Die Architektur eines Ein-Chip-Mikroprozessors mit eingebautem EEPROM wird vorgestellt. Die Leistung des EEPROM wird beschrieben, ebenso neue Anwendungen dieser Art Schaltungen.*

This paper has been presented at the Fall 1983 Meeting, of the IEEE Chapter on Solid-State Devices and Circuits October 1983, Bern. A similar paper had been presented at the ESSIRC 1982, Bruxelles.

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## 1. Introduction

In past years microprocessors were introduced with an on-chip UV erasable EPROM. This memory was generally provided for the development of the software, before the mass production of a mask programmed device. As these devices cannot be modified electrically, the range of applications is limited.

Simultaneously, new EEPROM devices were presented [1...4]. The process of these non-volatile electrically erasable devices evolved from the early P-channel MNOS EAROM to the recent N-channel floating polysilicon gate memories. These latter being process compatible with microprocessors, the integration of both devices on a single chip will bring new performances for many applications.

## 2. The Memory Cell

The memory cell [1] contains a select transistor in series with a FETMOS (Floating-Gate Electron Tunneling MOS) device. The FETMOS belongs to a new generation of EEPROM devices that relies on *Fowler-Nordheim* tunneling through a thin thermal oxide (12 nm) to charge and discharge the floating-gate. This type of EEPROM cell has the advantages of good data retention, good endurance [5], MPU compatible process and low power for program/write. The FETMOS utilizes the same active channel area as the tunneling area to achieve small cell size, high cell current and simple process. A cross section view of the device is shown in figure 1.

The positive threshold erased state is obtained by grounding the source, drain and substrate and raising the control-gate voltage to the programming supply voltage (20 V). Electron emission from the source, drain, and channel regions then charge the floating-gate to a more negative potential (fig. 2). The programmed state corresponds to a storage of positive charges on the floating-gate, resulting in a negative threshold as viewed from the control-gate. This state is obtained by tunneling electrons from the floating-gate to the N+ drain diffusion overlapped by the floating-gate. To program the device, the control-gate is grounded and the programming voltage is applied to the drain diffusion. A 10 V threshold voltage excursion is obtained which is centred about 0 V. Program and erase times are below 10 ms.

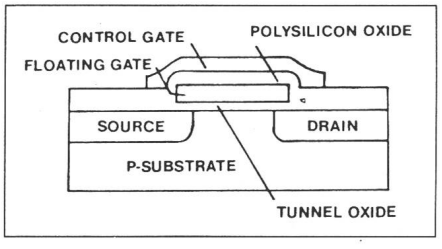
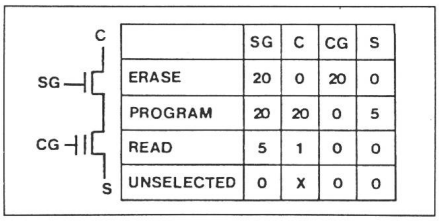



**Fig. 1 Memory transistor**




| | SG | C | CG | S |
|---|---|---|---|---|
| ERASE | 20 | 0 | 20 | 0 |
| PROGRAM | 20 | 20 | 0 | 5 |
| READ | 5 | 1 | 0 | 0 |
| UNSELECTED | 0 | X | 0 | 0 |

**Fig. 2 Operating modes of cell**
(applied voltage)

For read operation both the control-gate and the source of the memory device are held at VSS, and the drain at a low sensing voltage of about 1 V. These read conditions not only simplify memory array operation but also minimize the electrical stress accross the thin oxide. Therefore, unlimited read operations are possible. The FETMOS cell has demonstrated an endurance of over 100 k program/erase cycles as shown in figure 3.

The memory cell size is 375 $\mu m^2$, using feature size of 4 $\mu m$.

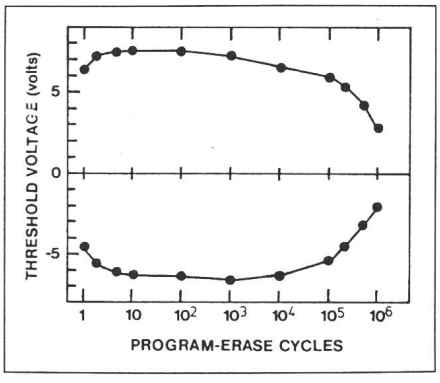



**Fig. 3 Program / erase endurance**

## 3. The Microcomputer

The microprocessor belongs to a standard 8 bits single chip microcomputer family. All the memories, input/output ports, and registers are memory mapped with the exception of the internal CPU registers. Therefore no distinction is made between memory used for program storage or for data storage. The advantage of this is clear when the function of the EEPROM has to be defined. In section 4 it will be shown that for some applications non-volatile data is needed, but other uses of this circuit will need reconfigurable software. This MPU family features 10 addressing modes, single instruction memory change and bit manipulation.

### *3.1 Microcomputer Block Diagram*

Figure 4 shows the block diagram of the single chip microcomputer. The CPU includes the control section and the operating section. The latter has a 12 bit program counter, two 8 bit registers A and X, a 5 bit condition code register, and a 5 bit stack pointer.

Four 8 bit wide input/output ports are provided. A serial port with 2 data lines, a clock and select line can be programmed in different full/half duplex and master/slave modes. Two 8 bit fully programmable timers can be cascaded or can have independent operation. Cascading these timers via software control enables the count of the relatively long write/erase times of the EEPROM (10 ms) with the internal 1 MHz clock.

The mask programmable ROM of 2 kbytes does not include the ROM used for self testing more than 90% of the chip. A 96 bytes RAM has 16 bytes powered via a special standby supply pin.

### *3.2 EEPROM Implementation*

There are different ways of implementing EEPROM memory on a microcomputer. This storage can be used either for program or for data.

For this low cost microcontroller it has been decided to include a mask programmable ROM as the device is targeted at large volume applications. (A ROM bit takes ⅓ of the area needed by an EEPROM bit.) But as all memories can be used for both data and program, it is possible to develop adaptive software where the EEPROM program will call pre-defined routines located in the ROM. For software compactness, the 128 bytes of EEPROM can be addressed by the shorter code of direct addressing instructions.

### *3.3 EEPROM Access*

As write and erase operations are much slower than the CPU operating speed, the address and the data are latched during these operations such that the MPU can perform other tasks. In read mode though, both latches are transparent and the memory access is similar to a ROM read.

To control these modes and other functions, an EEPROM control register contains up to 8 bits. Thus writing data to an address, erasing an address or the whole EEPROM is software controlled.

The family of MPUs has a test mode where both the internal address bus and data bus are visible on the I/O pins. In this mode, 2 bits of the EEPROM control register are used to verify the high and low EEPROM thresholds in conjunction with a variable voltage applied on a pin. This control register also includes a special EEPROM bit for protecting the data stored in the EEPROM in this test mode.

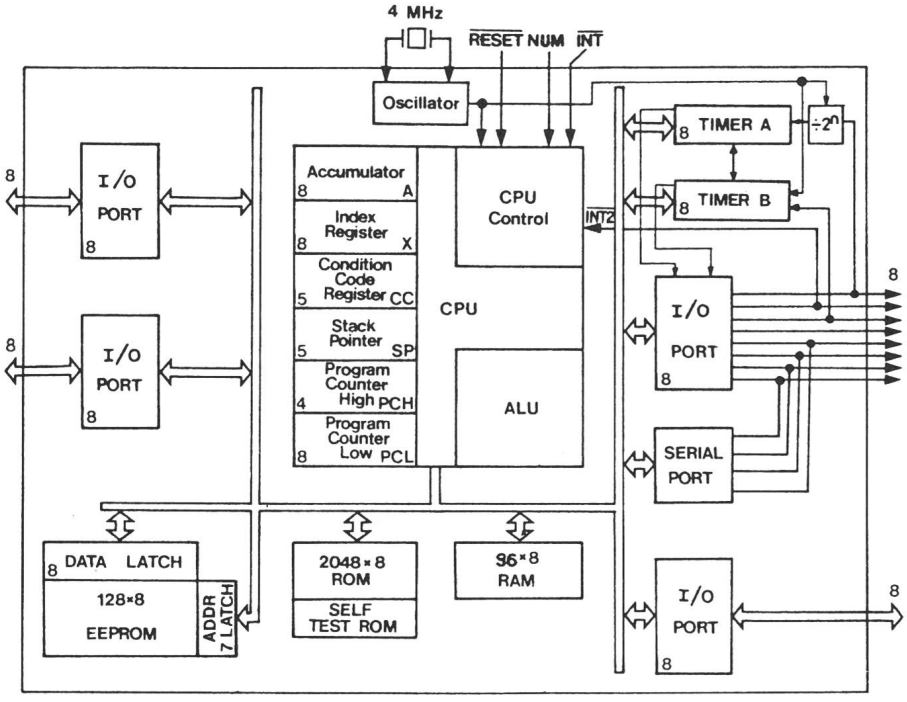



**Fig. 4 Microcomputer blockdiagram (MC 6805 K2)**

## 4. Applications

A MPU where an EEPROM is included on the same chip opens a entirely new field of applications. Many systems that were using a separate MPU and a non-volatile memory can now be realised at a lower cost.

For example, digital TV and radio tuning, programmable industrial process control, typewriter keyboards with adaptable character sets, recording of failure situations in safe parallel systems [6], and dashboard controller with odometer for automotive.

In this latest application an external non-volatile memory has a risk of data violation. An on-chip EEPROM with adequate software and hardware protection offers a safer approach. This is most important for data encription and data protection systems. In this case the encription key is stored in the EEPROM. The software will access the key within the single chip, preventing the user of seeing the encription key on a pin. This key can be reprogrammed electrically without removal from the system. The security EEPROM bit in the control register prevents an unwanted access to the key.

Self teaching systems can be developped where the sections of software in the EEPROM can be automatically or remotely modified.

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