Clock Device with Non-Volatile Memory Frequency Trimming

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Conventional electronic clock devices require an external capacitor for the frequency trimming of the quartz crystal. A device eliminating the capacitor has been produced. Non-volatile memory transistors fabricated in a normal CMOS process and their programming using voltage multipliers in the device are described. Device testing is described.

Bei Uhrenschaltungen wird normalerweise zum Trimmen des Quarzes (Frequenz) ein äusserer Kondensator benötigt. Es wird eine Schaltung vorgestellt, bei der dieser Kondensator umgangen werden kann. Dazu dienen nicht-flüchtige Speichertransistoren, die in einem gewöhnlichen CMOS-Prozess hergestellt und mittels Spannungsvervielfacher programmiert werden. Die Prüfung der Schaltung wird beschrieben.

Les circuits des montres électroniques comprennent normalement un condensateur extérieur pour ajuster la fréquence du quartz. Un dispositif qui permet d'éliminer ce condensateur a été conçu. Des transistors à mémoire non volatile fabriqués selon un procédé CMOS normal sont décrits ainsi que leur programmation au moyen d'un multiplicateur de tension et les tests du circuit.

1. Conventional Clock Device

The principle of operation of a conventional electronic clock device (block diagram in fig. 1) is to derive low-frequency pulses (normally 1 Hz) from a quartz crystal oscillator signal using dividers. 32-kHz crystals are commonly used (ie f = 32768 Hz). Crystal frequency tolerance is specified as frequency deviation in ppm (parts per million) with a certain series load capacitance. Typical tolerances are ± 15 ppm with a load capacitance of 10 pF. In order to achieve ± 2 ppm (approximately one minute accuracy a year) an external trimming capacitor is used to alter the quartz frequency. This value is sufficiently accurate in comparison to the temperature dependence of the quartz frequency. The frequency of oscillation can be shown to be given approximately by

$$f = f_s \left(1 + \frac{C_1}{2(C_0 + C_L)}\right)$$

where f_s is the series resonant frequency

C_1 the motional capacitance of the quartz
C_0 the static capacitance of the quartz
C_L the series load capacitance

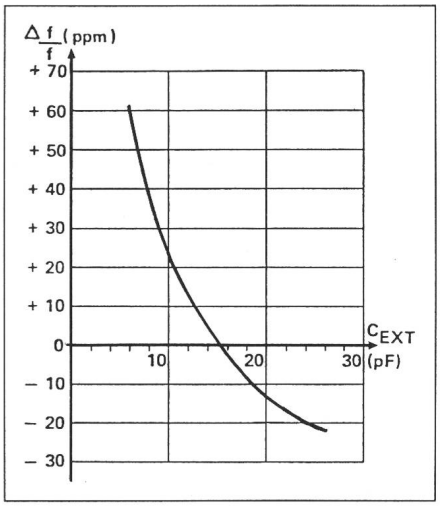

Fig. 2 Frequency deviation with external trimmer capacitance for a typical quartz
C_L = 10 pF, C_O = 1.1 pF, C_1 = 2.4 fF, C_{IN} = 2 pF, C_{OUT} = 24 pF

C_L is given approximately by

$$C_L = \frac{C_{out}(C_{in} + C_{ext})}{C_{out} + C_{in} + C_{ext}}$$

where C_{out} is the capacitance at the oscillator output
C_{in} the stray capacitance at the oscillator input
C_{ext} the external trimmer capacitance at the oscillator input

Figure 2 shows the relationship between frequency deviation and external

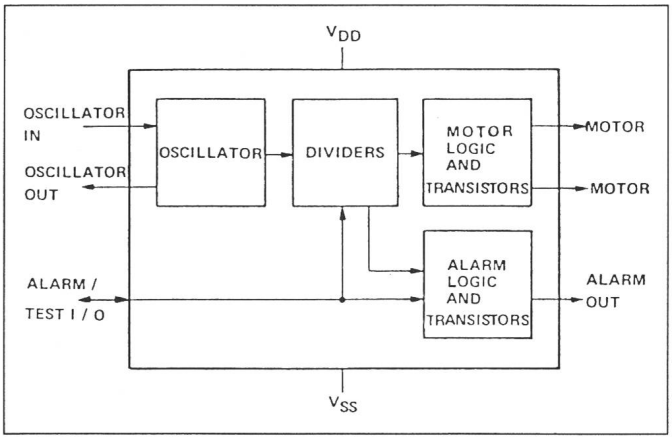

Fig. 1 Block diagram of a conventional clock device (8 pin)

This paper has been presented at the Fall 1983 Meeting, of the IEEE Chapter on Solid-State Devices and Circuits, October 1983, Bern. Part of this project was supported by the Swiss «Impulsprogramm».

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capacitance C_{ext} for a typical quartz crystal.

2. New Device

A device has been produced which eliminates the external trimming capacitor by containing a programmable on-chip capacitor. The device is pin compatible with the conventional device. The data is stored in non-volatile memory FAMOS (floating-gate Avalanche MOS) transistors.

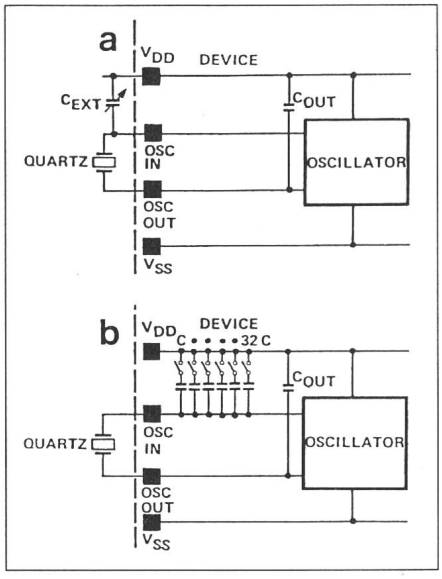

Fig. 3 Replacing the external capacitor with an on-chip programmable capacitor

a conventional oscillator circuit
b new oscillator circuit

Figure 3 shows the oscillator diagram for a conventional device and the new device. The programmable capacitor has six binary valued capacitances giving 64 steps similar to a discrete trimmer. The idealised switches are actually realized with low-resistance transistors driven by data in six FAMOS transistors. Trimming is performed by the clock manufacturer by measuring the quartz frequency and programming the capacitor. The advantages of the new device are

a) a reduction in the number of components needed,
b) improved reliability of the trimmer capacitance,
c) a faster, all-electronic trimming procedure.

2.1 FAMOS Transistors

FAMOS transistors store data as electronic charge in an insulated polysilicon gate. With sufficient negative charge the p-type transistor is on, otherwise it is off. Figure 4 is a photograph of the FAMOS transistor fabricated in a normal 6-mask CMOS process whose basic design was done at CEH (Centre Electronique Horloger, Neuchâtel). The transistor with n-type substrate comprises a floating gate of polysilicon with a metal control gate above it, a p-type transistor formed with part of the floating gate (left), a separate p-type region (right) and a gate oxide region (middle). The operation of the device is fully explained in [1]. To turn the transistor on (called Writing) approximately -32 V is applied to the separate p-type region called the injector, whereby electrons are injected and energetically trapped in the floating gate. To turn off the transistor (called Erasing) approximately -80 V is applied to the control gate, whereby electrons are emitted by tunneling through the gate oxide region to the substrate. Gate oxide is 65 nm thick. The transistors are programmed using on-chip voltage multipliers.

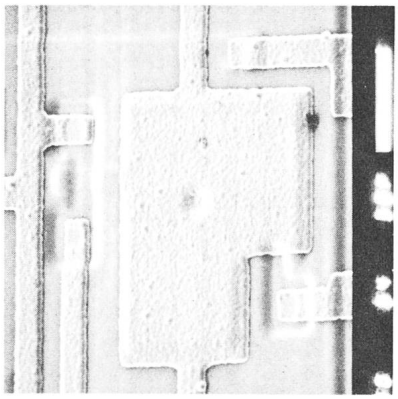

Fig. 4 Photograph of a FAMOS transistor

2.2 Data Input

The data is input serially at the test pin using pulses beyond the supply voltage and a special input circuit. Six serially connected dividers perform serial to parallel conversion, with the last divider outputing the most significant bit for the largest capacitor. The data switches the appropriate capacitors to allow remeasurement of the quartz frequency until sufficient accuracy is achieved.

2.3 Voltage Multipliers

Each FAMOS transistor has a voltage multiplier for generating the write voltage and all six transistors a common voltage multiplier to generate the erase voltage. Erasure is necessary for testing. Figure 5 shows the circuit diagram for two stages of the voltage multipliers whose principle of operation, charge pumping, is explained in [2]. Diodes are formed in polysilicon and capacitors with polysilicon and metal. The output voltage is approximately given by

$$V_{out} = -n(V_{supply} - 2\,V_D)$$

where n is the number of stages and V_D is a diode-voltage drop.

To store data after data input the supply voltage (normally 1.5 V) is increased to 5.5 V and a 1-MHz signal is applied to the Alarm-out pin. The number of stages needed in the multipliers is therefore kept low. Advantages of using voltage multipliers are:

a) The FAMOS cells are isolated from the pins preventing data loss due to spurious high voltages due to device handling.
b) Programming is easier (no high voltages).

Figure 6 shows a photograph of the device.

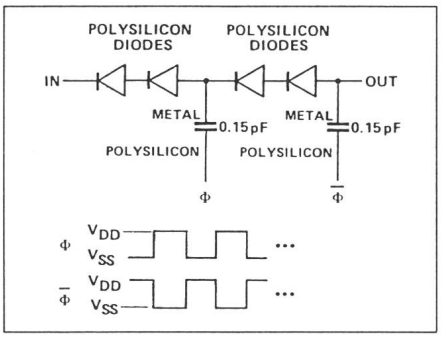

Fig. 5 Two stages of the voltage multiplier

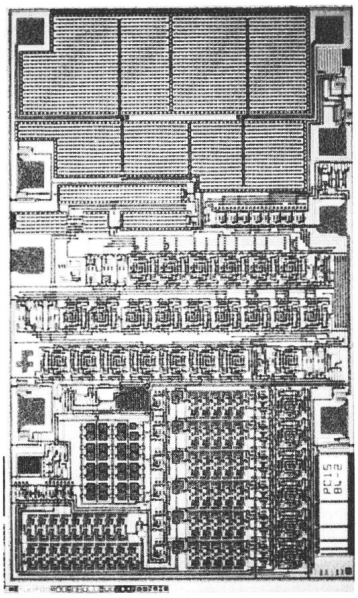

Fig. 6 Photograph of the device

3. Data Retention

To ensure correct operation of the device the charge stored in the floating gates of the FAMOS transistors must remain for a long period of time. Measurements on single FAMOS transistors show two effects:

a) A slight loss of charge occurs shortly after programming (within hours).
b) A gradual loss of charge occurs over a long time period (within years).

The first effect is thought due to charges which are not properly trapped, and can be taken into account by having a sufficient reserve of charge. The relatively thick oxide of 65 nm is expected to give a long data retention time. Measurements at high temperature accelerate charge loss. Measurements on FAMOS devices over periods of 10 to 30 days at 170 °C indicate that at 100 °C sufficient charge will still remain after at least 12 to 700 years based on worst and best-case estimates respectively. A retention time of 10 years at 60 °C maximum can therefore be expected to be easily achieved.

4. Device Testing in Production

The basis of testing the FAMOS transistors lies in the known relationship between the amount of charge in the floating gate and the programming voltages known approximately from the supply voltage. By testing writing and erasing with lower supply voltages than specified one can ensure a reserve of charge when programmed by the clock manufacturer and take the short-term charge loss into account. Furthermore every FAMOS transistor goes through a data retention test by writing on the wafer and checking after assembly. Several high-temperature steps are involved including ½ hour at 200 °C, 1 hour at 260 °C and 16 hours at 160 °C. In this way possible defect FAMOS transistors may be detected.

The device is now in production and information is available from any Philips Sales Office.

References

[1] *E. Gerber* and *J. Fellrath:* Low-voltage single supply CMOS electrically erasable read-only memory. IEEE Trans. ED 27(1980)7, p. 1211...1216.

[2] *J.F. Dickson:* On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. IEEE Journal of Solid-State Circuits 11(1976)3, p. 374...378.